RPS-9X-PS

SpaceVPX Reprogrammable Processor System 9-slot eXtensible

Version #: 1.0.4

12/24/2024

Introduction

The Frontgrade™ Reprogrammable Processing System™ 9-slot eXtensible (RPS-9X-PS) includes the SpaceVPX Reprogrammable Processing Module (RPM-PS) with an AMD/Xilinx® XQR-Grade VC1902 System-on-Chip (SoC) with dual A72 ARM cores (up to 1.7 GHz) and dual Cortex-R5 cores for up to 3 instances across Slot 1 to Slot 3. Programmable logic may be implemented by the end user to allow high-throughput SpaceWire and Ethernet data switching. The compact 160mm 3U design with a customizable mezzanine (Frontgrade's IOM-PS) allows for tailoring I/O to meet program requirements. Provides high speed data at up to 10 Gbps between processors and the 8-port Ethernet I/O module (Frontgrade's SEIM-PS) in Slot 4. An RF Tx/Rx module (Frontgrade's SRFM-PS) provides direct-to-digital conversion of L/S-band signals using Slot 5 to the RPM in Slot 2 for signal processing and converted analog output to RF up/downlink. The optional RPM in Slot 3 can provide additional I/Os to a spare I/O module in Slot 6. The development dongle is available to access the I/O on each RPM using JTAG, UART, or 1000Base-T Ethernet for software development.

Features

Processing / Data Rates / Connectivity:

- Processor: Versal® VC1902 System-on-Chip (SoC) with dual A72 ARM™ cores (up to 1.7 GHz) and dual Cortex-R5® cores (up to 750 MHz)
- Volatile Memory: 16 GB DDR4 memory
- Non-Volatile Boot Memory: 8 Gbits QSPI memory
- Non-Volatile Storage: 1Tb maximum of raw data storage in SLC mode

When Configured With The RPS™ Mezzanine Card In Any RPM Slot:

- Three 100Base-TX and one 1000Base-T ports
- One SpaceWire port of up to 200 Mbps per port and two RS422 UARTs up to 115.2 kbps
- Discrete IOs: 1x LVDS inputs, 2x LVDS pulse output, 1x LVDS SPI, 1x LVTTL/LVCMOS input, 1x LVTTL/LVCMOS output
- For each RPM front panel, two SGMII Current Model Logic (CML) channels at 1.25 Gbauds per second per channel
- Slot 4 Ethernet I/O module offers up to eight 1000/2.5G/5G/10GBase-T ports (same data rate for every four ports)
- Slot 5 one Analog RF input with a 12-bit ADC and one Analog RF output with a 16-bit DAC

Mass / Volume / Thermal:

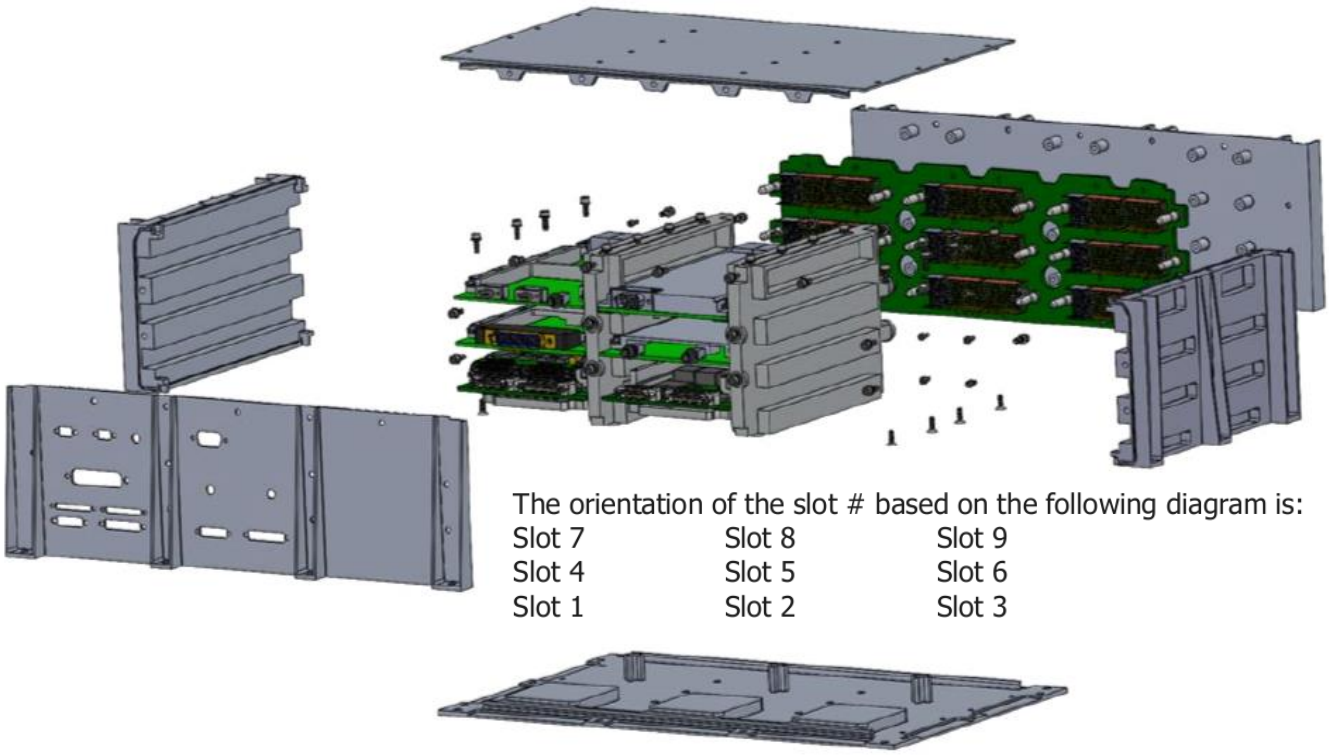
- Mass: less than 10 kg (estimated)
- Dimensions: 13.75" (L) x 8.25" (W) x 4.2" (H), ICD including mounting hole pattern
- Maximum operating temperature mounted on a regulated thermal interface: 52°C
- Maximum power consumption: 300W with 288W output for all slots including the two RPMs (80W maximum for each Versal SoC 0.8 Vdc core voltage depending on the dynamic power utilization for all cards as a system)

Operational Life/Reliability and Performance (With Two Rpms):

- System reliability over 0.87
- System SEU rate: No more than one per 10 months for typical LEO Missions
- TID of 25 krads (Si) or 100 krads (Si) optional assuming 100 mils of shielding with 6061-T6 Aluminum
- Level-2 parts pedigree per EEE-INST-002 and PEM-INST-001 is available

Development Environment:

- Separate development dongle for interface with SmartLynq+ System Debugger
- Vivado® 2023.2 development environment with PetaLinux Linux Support Package (LSP)



The orientation of the slot # based on the following diagram is:

Slot 7	Slot 8	Slot 9
Slot 4	Slot 5	Slot 6
Slot 1	Slot 2	Slot 3