# Using Bus Switches to Enable 50 krad(Si) Total Ionizing Dose Performance on the UT8QNF8M8 64Mbit NOR Flash Memory

DESIGN NOTE

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## 1. Introduction

The UT8QNF8M8 64Mbit NOR Flash Memory specifies a maximum total ionizing dose of 50 krad(Si) in an operational environment where the device is unpowered for 90% of its mission life. This kind of environment matches with the mission profile where the NOR Flash is used as boot load memory. In this application, the NOR Flash is only accessed during system power up and reset, and could be powered down for the rest of the mission. This unpowered state can be achieved by powering the NOR Flash through a combination of bus switch products.

## 2. Design Implementation

Figure 1 depicts a block diagram connecting the memory controller of the UT700 LEON 3FT processor to a UT8QNF8M8 64Mbit NOR Flash through a UT54BS16245 16-Bit 1:1 Bus Switch and a UT54BS32245 32-Bit 1:1 Bus Switch. The bus switches provide isolation for the NOR flash inputs, as well as a switching mechanism for the NOR Flash VCC power supply. 1:1 bus switches provide a per channel off resistance greater than 1 MΩ when disabled and a typical on resistance of less than 10Ω when operated in the 3.3V supply range. Each channel allows 60mA continuous current, providing significant margin to the 30mA maximum supply current specified for the NOR Flash during program and erase.

On the NOR Flash, the Byte# pin is tied low which places the memory into byte mode and tri-states pins DQ[14:8] and sets DQ15 to A-1 (LSB address pin). This frees 8 channels on the 16-bit switch to connect VDD to NOR Flash VCC. The combined eight channels add a worst case 2Ω series resistance resulting in a maximum 60mV drop under worst case program/erase conditions. VDD power supply should be set to a range of nominal +-5% to account for this drop.

The NOR Flash control pins, (CE#, OE#, WE#, and RESET#) are tied to VCC through 1KΩ resistors to ensure that the part is not inadvertently enabled. In addition, a 1nF decoupling capacitor should be placed at the NOR Flash VCC to account for high speed access operations.

The LEON memory controller controls the bus switch enable pins using GPIO[3], and the application pulls these pins high to disable the Flash memory after data is transferred to a volatile memory location. During a processor reset, GPIO[3] will be in a high-z state and the 1KΩ pull down on the enable pins ensures that the NOR Flash will be available when the reset is complete. Redundancy could be added to this by using additional GPIO pins through an OR gate.

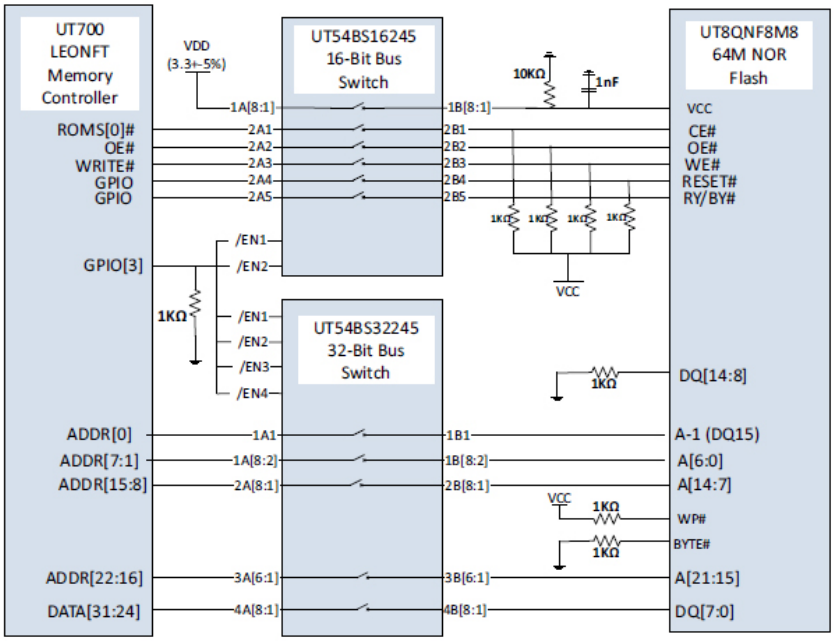


**Figure 1. Example Bus Switch\NOR Flash Configuration**

## 3. Conclusion

The UT8QNF8M8 64Mbit NOR Flash provides a simple way of storing memory during boot up operations, and the design described in this note enables the user to achieve the NOR Flash full 50 krad(Si) specification.