32, 64, 128 Megabit SRAM MCM

# UT8ER1M32, UT8ER2M32, UT8ER4M32

## Features

- 20ns Read, 10ns Write maximum access times available
- Functionally compatible with traditional 1M, 2M and 4M x 32 SRAM devices
- CMOS compatible input and output levels, three-state bidirectional data bus
  - I/O Voltages 2.3V to 3.6V, 1.7V to 2.0Vcore
- Available densities:
  - UT8ER1M32: 33, 554, 432 bits
  - UT8ER2M32: 67, 108, 864 bits
  - UT8ER4M32: 134, 217, 728 bits
- Operational environment:
  - Total-dose: 100 krad (Si)
  - SEL Immune: $\leq110$ MeV-cm$^2$/mg
  - SEU error rate = 8.1 x10$^{-16}$ errors/bit-day assuming geosynchronous orbit, Adam's 90% worst environment, and 6600ns default Scrub Rate Period (=97% SRAM availability)
- Packaging option:
  - 132-lead side-brazed dual cavity ceramic quad flatpack
- Standard Microelectronics Drawing:
  - UT8ER1M32: 5962-10202
    - QML Q, Q+ and V compliant
  - UT8ER2M32: 5962-10203
    - QML Q, Q+, and V compliant
  - UT8ER4M32: 5962-10204
    - QML Q and Q+ compliant

## Introduction

The UT8ER1M32, UT8ER2M32, and UT8ER4M32 are high performance CMOS static RAM multichip modules (MCMs) organized as two, four or eight individual 524,288 words x 32 bits dice respectively. Easy memory expansion is provided by active LOW chip enables ($\overline{En}$), an active LOW output enable ($\overline{G}$), and three-state drivers. This device has a power-down feature that reduces power consumption by more than 90% when deselected. Autonomous (master) and demanded (slave) scrubbing continues while deselected.

Writing to the device is accomplished by driving one of the chip enable ($\overline{En}$) inputs LOW and the write enable ($\overline{W}$) input LOW. Data on the 32 I/O pins (DQ0 through DQ31) is then written into the location specified on the address pins (A0 through A18). Reading from the device is accomplished by driving one of the chip enables ($\overline{En}$) and output enable ($\overline{G}$) LOW while driving write enable ($\overline{W}$) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins. **Note:** Only on $\overline{En}$ pin may be active at any time.

The 32 input/output pins (DQ0 through DQ31) are placed in a high impedance state when the device is deselected ($\overline{En}$ HIGH), the outputs are disabled ($\overline{G}$ HIGH), or during a write operation ($\overline{En}$ LOW, $\overline{W}$ LOW)

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## Block Diagram



Figure 1. Block Diagram

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32M /64M/ 128M
2-, 4-, 8- Die
SRAM MCM Module

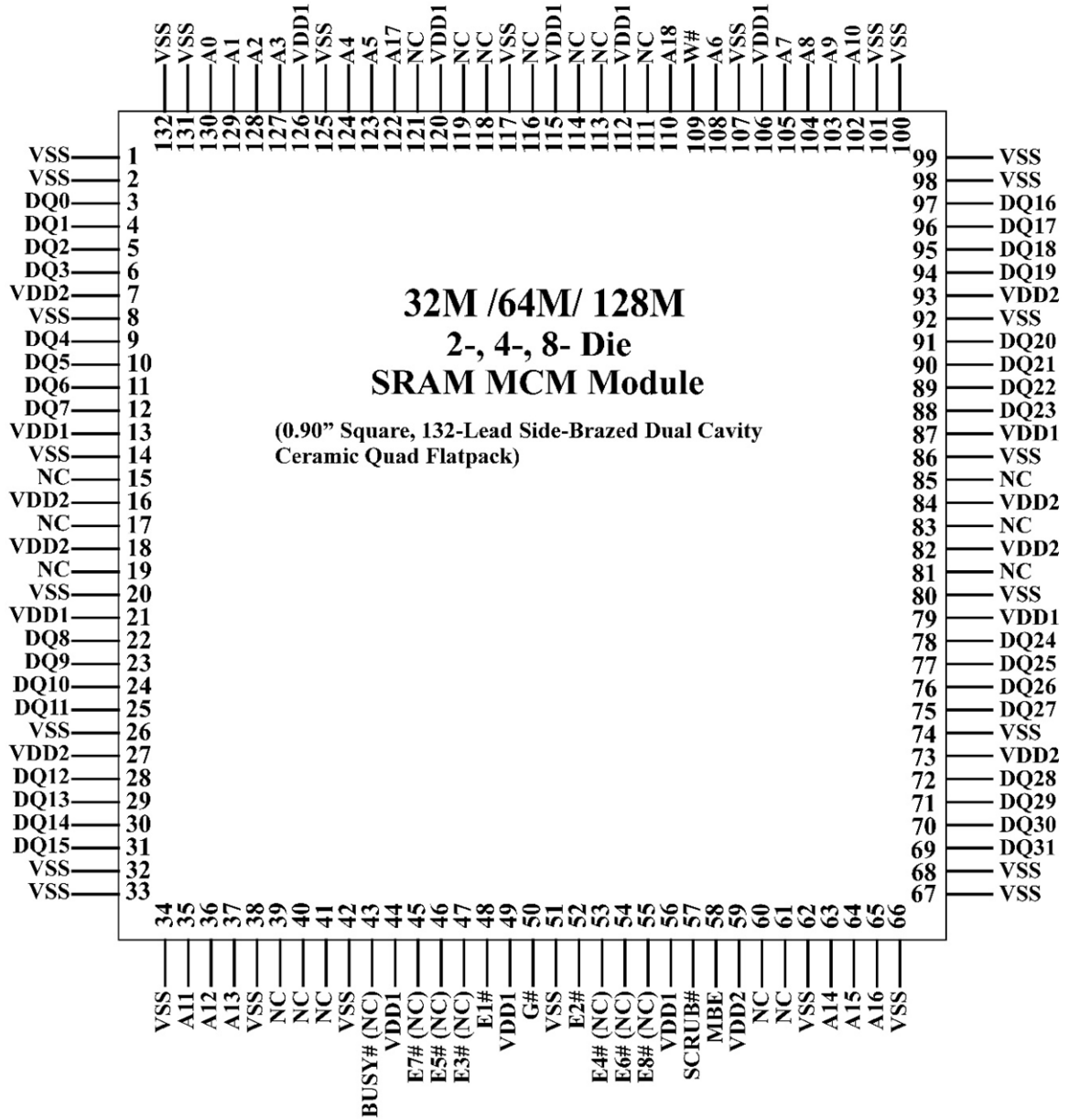(0.90" Square, 132-Lead Side-Brazed Dual Cavity
Ceramic Quad Flatpack)
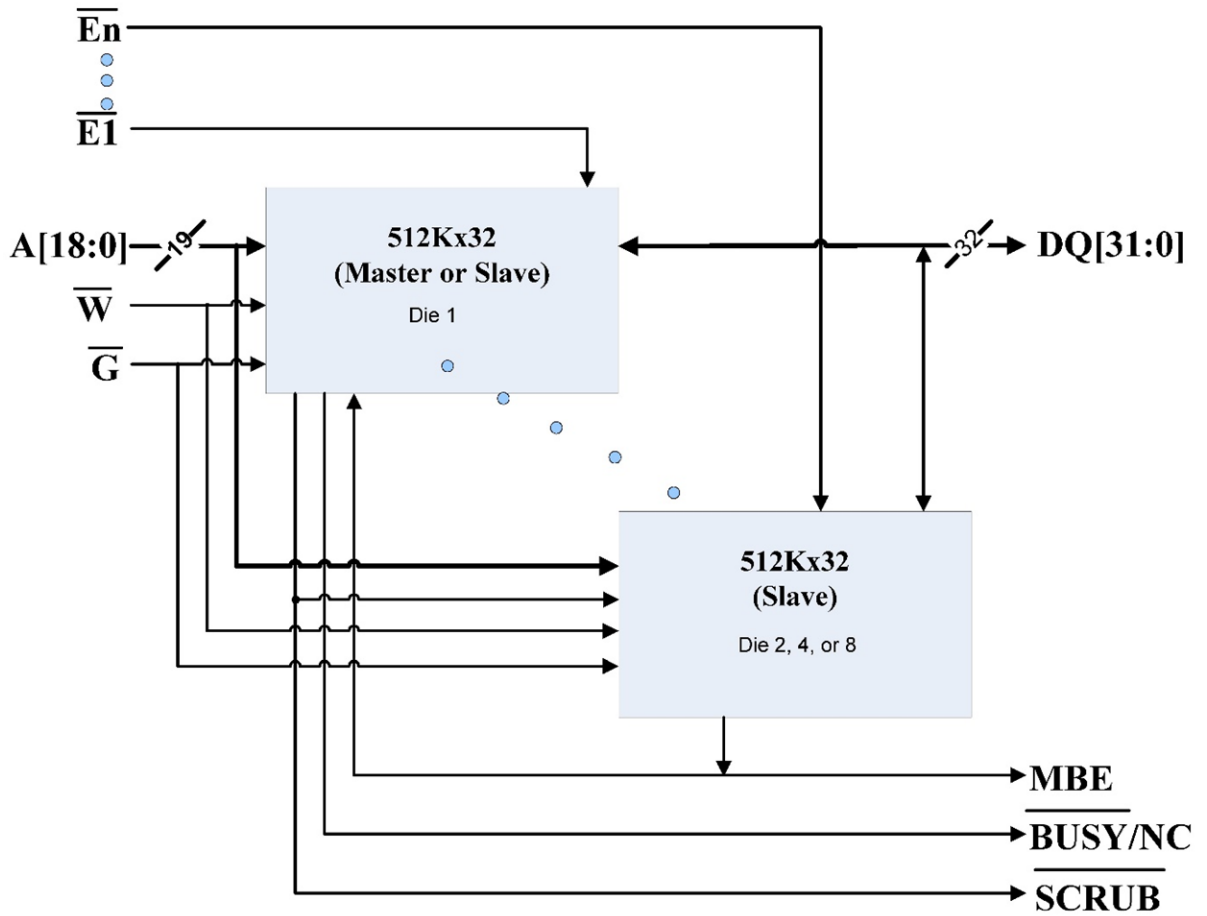
Figure 2. Pin Diagram

**Notes:**

1) NC = Pins are not connected on die.

2) (NC) = Depending on device option, pin may be either signal as named or NC (see Table 1).

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# UT8ER1M32, UT8ER2M32, UT8ER4M32

## Table 1.  Pin Description

| Pin | Type | Description |
|---|---|---|
| A(18:0) | I | Address Input |
| DQ(31:0) | BI | Data Input/Output |
| En#* | I | Enable (Active Low) |
| W# | I | Write Enable (Active Low) |
| G# | I | Output Enable (Active Low) |
| VDD1 | P | Power (1.8V nominal) |
| VDD2 | P | Power (3.3V nominal) |
| VSS | P | Ground |
| MBE | BI | Multiple Bit Error |
| SCRUB# | I | Slave SCRUB Input (Active Low) |
| SCRUB# | O | Master SCRUB Output |
| BUSY# | NC | Slave No Connect |
| BUSY# | O | Master Wait State Control |

**Notes**:

* n represents any number of individual MCM (multichip module) die enables. May be 1-8 depending on device option.

## Table 2. Device Option: Signal and Pin Description

| Pkg Pin # | UT8ER1M32M (Master) Signal Name | UT8ER1M32S (Slave) Signal Name | UT8ER2M32M (Master) Signal Name | UT8ER2M32S (Slave) Signal Name | UT8ER4M32M (Master) Signal Name | UT8ER4M32S (Slave) Signal Name | Device Pin Description |
|---|---|---|---|---|---|---|---|
| 1 | VSS | VSS | VSS | VSS | VSS | VSS | PWR |
| 2 | VSS | VSS | VSS | VSS | VSS | VSS | PWR |
| 3 | DQ0 | DQ0 | DQ0 | DQ0 | DQ0 | DQ0 | DATA I/O |
| 4 | DQ1 | DQ1 | DQ1 | DQ1 | DQ1 | DQ1 | DATA I/O |
| 5 | DQ2 | DQ2 | DQ2 | DQ2 | DQ2 | DQ2 | DATA I/O |
| 6 | DQ3 | DQ3 | DQ3 | DQ3 | DQ3 | DQ3 | DATA I/O |
| 7 | VDD2 | VDD2 | VDD2 | VDD2 | VDD2 | VDD2 | PWR |
| 8 | VSS | VSS | VSS | VSS | VSS | VSS | PWR |
| 9 | DQ4 | DQ4 | DQ4 | DQ4 | DQ4 | DQ4 | DATA I/O |
| 10 | DQ5 | DQ5 | DQ5 | DQ5 | DQ5 | DQ5 | DATA I/O |
| 11 | DQ6 | DQ6 | DQ6 | DQ6 | DQ6 | DQ6 | DATA I/O |
| 12 | DQ7 | DQ7 | DQ7 | DQ7 | DQ7 | DQ7 | DATA I/O |
| 13 | VDD1 | VDD1 | VDD1 | VDD1 | VDD1 | VDD1 | PWR |
| 14 | VSS | VSS | VSS | VSS | VSS | VSS | PWR |
| 15 | NC | NC | NC | NC | NC | NC | NC |
| 16 | VDD2 | VDD2 | VDD2 | VDD2 | VDD2 | VDD2 | PWR |
| 17 | NC | NC | NC | NC | NC | NC | NC |
| 18 | VDD2 | VDD2 | VDD2 | VDD2 | VDD2 | VDD2 | PWR |
| 19 | NC | NC | NC | NC | NC | NC | NC |
| 20 | VSS | VSS | VSS | VSS | VSS | VSS | PWR |

# UT8ER1M32, UT8ER2M32, UT8ER4M32

**Table 2. Device Option: Signal and Pin Description (Cont'd)**

| Pkg Pin # | UT8ER1M32M (Master) Signal Name | UT8ER1M32S (Slave) Signal Name | UT8ER2M32M (Master) Signal Name | UT8ER2M32S (Slave) Signal Name | UT8ER4M32M (Master) Signal Name | UT8ER4M32S (Slave) Signal Name | Device Pin Description |
|---|---|---|---|---|---|---|---|
| 21 | VDD1 | VDD1 | VDD1 | VDD1 | VDD1 | VDD1 | PWR |
| 22 | DQ8 | DQ8 | DQ8 | DQ8 | DQ8 | DQ8 | DATA I/O |
| 23 | DQ9 | DQ9 | DQ9 | DQ9 | DQ9 | DQ9 | DATA I/O |
| 24 | DQ10 | DQ10 | DQ10 | DQ10 | DQ10 | DQ10 | DATA I/O |
| 25 | DQ11 | DQ11 | DQ11 | DQ11 | DQ11 | DQ11 | DATA I/O |
| 26 | VSS | VSS | VSS | VSS | VSS | VSS | PWR |
| 27 | VDD2 | VDD2 | VDD2 | VDD2 | VDD2 | VDD2 | PWR |
| 28 | DQ12 | DQ12 | DQ12 | DQ12 | DQ12 | DQ12 | DATA I/O |
| 29 | DQ13 | DQ13 | DQ13 | DQ13 | DQ13 | DQ13 | DATA I/O |
| 30 | DQ14 | DQ14 | DQ14 | DQ14 | DQ14 | DQ14 | DATA I/O |
| 31 | DQ15 | DQ15 | DQ15 | DQ15 | DQ15 | DQ15 | DATA I/O |
| 32 | VSS | VSS | VSS | VSS | VSS | VSS | PWR |
| 33 | VSS | VSS | VSS | VSS | VSS | VSS | PWR |
| 34 | VSS | VSS | VSS | VSS | VSS | VSS | PWR |
| 35 | A11 | A11 | A11 | A11 | A11 | A11 | ADDRESS INPUT |
| 36 | A12 | A12 | A12 | A12 | A12 | A12 | ADDRESS INPUT |
| 37 | A13 | A13 | A13 | A13 | A13 | A13 | ADDRESS INPUT |
| 38 | VSS | VSS | VSS | VSS | VSS | VSS | PWR |
| 39 | NC | NC | NC | NC | NC | NC | NC |
| 40 | NC | NC | NC | NC | NC | NC | NC |
| 41 | NC | NC | NC | NC | NC | NC | NC |
| 42 | VSS | VSS | VSS | VSS | VSS | VSS | PWR |
| 43 | BUSY# | NC | BUSY# | NC | BUSY# | NC | OUTPUT[1] |
| 44 | VDD1 | VDD1 | VDD1 | VDD1 | VDD1 | VDD1 | PWR |
| 45 | NC | NC | NC | NC | E7# | E7# | CONTROL INPUT[2] |
| 46 | NC | NC | NC | NC | E5# | E5# | CONTROL INPUT[2] |
| 47 | NC | NC | E3# | E3# | E3# | E3# | CONTROL INPUT[2] |
| 48 | E1# | E1# | E1# | E1# | E1# | E1# | CONTROL INPUT |
| 49 | VDD1 | VDD1 | VDD1 | VDD1 | VDD1 | VDD1 | PWR |
| 50 | G# | G# | G# | G# | G# | G# | CONTROL INPUT |
| 51 | VSS | VSS | VSS | VSS | VSS | VSS | PWR |
| 52 | E2# | E2# | E2# | E2# | E2# | E2# | CONTROL INPUT |

**Table 2. Device Option: Signal and Pin Description (Cont'd)**

| Pkg Pin # | UT8ER1M32M (Master) Signal Name | UT8ER1M32S (Slave) Signal Name | UT8ER2M32M (Master) Signal Name | UT8ER2M32S (Slave) Signal Name | UT8ER4M32M (Master) Signal Name | UT8ER4M32S (Slave) Signal Name | Device Pin Description |
|---|---|---|---|---|---|---|---|
| 53 | NC | NC | E4# | E4# | E4# | E4# | CONTROL INPUT[2] |
| 54 | NC | NC | NC | NC | E6# | E6# | CONTROL INPUT[2] |
| 55 | NC | NC | NC | NC | E8# | E8# | CONTROL INPUT[2] |
| 56 | VDD1 | VDD1 | VDD1 | VDD1 | VDD1 | VDD1 | PWR |
| 57 | SCRUB# | SCRUB# | SCRUB# | SCRUB# | SCRUB# | SCRUB# | CONTROL I/O[3] |
| 58 | MBE | MBE | MBE | MBE | MBE | MBE | DATA I/O |
| 59 | VDD2 | VDD2 | VDD2 | VDD2 | VDD2 | VDD2 | PWR |
| 60 | NC | NC | NC | NC | NC | NC | NC |
| 61 | NC | NC | NC | NC | NC | NC | NC |
| 62 | VSS | VSS | VSS | VSS | VSS | VSS | PWR |
| 63 | A14 | A14 | A14 | A14 | A14 | A14 | ADDRESS INPUT |
| 64 | A15 | A15 | A15 | A15 | A15 | A15 | ADDRESS INPUT |
| 65 | A16 | A16 | A16 | A16 | A16 | A16 | ADDRESS INPUT |
| 66 | VSS | VSS | VSS | VSS | VSS | VSS | PWR |
| 67 | VSS | VSS | VSS | VSS | VSS | VSS | PWR |
| 68 | VSS | VSS | VSS | VSS | VSS | VSS | PWR |
| 69 | DQ31 | DQ31 | DQ31 | DQ31 | DQ31 | DQ31 | DATA I/O |
| 70 | DQ30 | DQ30 | DQ30 | DQ30 | DQ30 | DQ30 | DATA I/O |
| 71 | DQ29 | DQ29 | DQ29 | DQ29 | DQ29 | DQ29 | DATA I/O |
| 72 | DQ28 | DQ28 | DQ28 | DQ28 | DQ28 | DQ28 | DATA I/O |
| 73 | VDD2 | VDD2 | VDD2 | VDD2 | VDD2 | VDD2 | PWR |
| 74 | VSS | VSS | VSS | VSS | VSS | VSS | PWR |
| 75 | DQ27 | DQ27 | DQ27 | DQ27 | DQ27 | DQ27 | DATA I/O |
| 76 | DQ26 | DQ26 | DQ26 | DQ26 | DQ26 | DQ26 | DATA I/O |
| 77 | DQ25 | DQ25 | DQ25 | DQ25 | DQ25 | DQ25 | DATA I/O |
| 78 | DQ24 | DQ24 | DQ24 | DQ24 | DQ24 | DQ24 | DATA I/O |
| 79 | VDD1 | VDD1 | VDD1 | VDD1 | VDD1 | VDD1 | PWR |
| 80 | VSS | VSS | VSS | VSS | VSS | VSS | PWR |
| 81 | NC | NC | NC | NC | NC | NC | NC |
| 82 | VDD2 | VDD2 | VDD2 | VDD2 | VDD2 | VDD2 | PWR |
| 83 | NC | NC | NC | NC | NC | NC | NC |
| 84 | VDD2 | VDD2 | VDD2 | VDD2 | VDD2 | VDD2 | PWR |
| 85 | NC | NC | NC | NC | NC | NC | NC |
| 86 | VSS | VSS | VSS | VSS | VSS | VSS | PWR |
| 87 | VDD1 | VDD1 | VDD1 | VDD1 | VDD1 | VDD1 | PWR |
| 88 | DQ23 | DQ23 | DQ23 | DQ23 | DQ23 | DQ23 | DATA I/O |
| 89 | DQ22 | DQ22 | DQ22 | DQ22 | DQ22 | DQ22 | DATA I/O |

# UT8ER1M32, UT8ER2M32, UT8ER4M32

**Table 2. Device Option: Signal and Pin Description (Cont'd)**

| Pkg Pin # | UT8ER1M32M (Master) Signal Name | UT8ER1M32S (Slave) Signal Name | UT8ER2M32M (Master) Signal Name | UT8ER2M32S (Slave) Signal Name | UT8ER4M32M (Master) Signal Name | UT8ER4M32S (Slave) Signal Name | Device Pin Description |
|---|---|---|---|---|---|---|---|
| 90 | DQ21 | DQ21 | DQ21 | DQ21 | DQ21 | DQ21 | DATA I/O |
| 91 | DQ20 | DQ20 | DQ20 | DQ20 | DQ20 | DQ20 | DATA I/O |
| 92 | VSS | VSS | VSS | VSS | VSS | VSS | PWR |
| 93 | VDD2 | VDD2 | VDD2 | VDD2 | VDD2 | VDD2 | PWR |
| 94 | DQ19 | DQ19 | DQ19 | DQ19 | DQ19 | DQ19 | DATA I/O |
| 95 | DQ18 | DQ18 | DQ18 | DQ18 | DQ18 | DQ18 | DATA I/O |
| 96 | DQ17 | DQ17 | DQ17 | DQ17 | DQ17 | DQ17 | DATA I/O |
| 97 | DQ16 | DQ16 | DQ16 | DQ16 | DQ16 | DQ16 | DATA I/O |
| 98 | VSS | VSS | VSS | VSS | VSS | VSS | PWR |
| 99 | VSS | VSS | VSS | VSS | VSS | VSS | PWR |
| 100 | VSS | VSS | VSS | VSS | VSS | VSS | PWR |
| 101 | VSS | VSS | VSS | VSS | VSS | VSS | PWR |
| 102 | A10 | A10 | A10 | A10 | A10 | A10 | ADDRESS INPUT |
| 103 | A9 | A9 | A9 | A9 | A9 | A9 | ADDRESS INPUT |
| 104 | A8 | A8 | A8 | A8 | A8 | A8 | ADDRESS INPUT |
| 105 | A7 | A7 | A7 | A7 | A7 | A7 | ADDRESS INPUT |
| 106 | VDD1 | VDD1 | VDD1 | VDD1 | VDD1 | VDD1 | PWR |
| 107 | VSS | VSS | VSS | VSS | VSS | VSS | PWR |
| 108 | A6 | A6 | A6 | A6 | A6 | A6 | ADDRESS INPUT |
| 109 | W# | W# | W# | W# | W# | W# | CONTROL INPUT |
| 110 | A18 | A18 | A18 | A18 | A18 | A18 | ADDRESS INPUT |
| 111 | NC | NC | NC | NC | NC | NC | NC |
| 112 | VDD1 | VDD1 | VDD1 | VDD1 | VDD1 | VDD1 | PWR |
| 113 | NC | NC | NC | NC | NC | NC | NC |
| 114 | NC | NC | NC | NC | NC | NC | NC |
| 115 | VDD1 | VDD1 | VDD1 | VDD1 | VDD1 | VDD1 | PWR |
| 116 | NC | NC | NC | NC | NC | NC | NC |
| 117 | VSS | VSS | VSS | VSS | VSS | VSS | PWR |
| 118 | NC | NC | NC | NC | NC | NC | NC |
| 119 | NC | NC | NC | NC | NC | NC | NC |
| 120 | VDD1 | VDD1 | VDD1 | VDD1 | VDD1 | VDD1 | PWR |
| 121 | NC | NC | NC | NC | NC | NC | NC |
| 122 | A17 | A17 | A17 | A17 | A17 | A17 | ADDRESS INPUT |

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# UT8ER1M32, UT8ER2M32, UT8ER4M32

**Table 2. Device Option: Signal and Pin Description (Cont'd)**

| Pkg Pin # | UT8ER1M32M (Master) Signal Name | UT8ER1M32S (Slave) Signal Name | UT8ER2M32M (Master) Signal Name | UT8ER2M32S (Slave) Signal Name | UT8ER4M32M (Master) Signal Name | UT8ER4M32S (Slave) Signal Name | Device Pin Description |
|---|---|---|---|---|---|---|---|
| 123 | A5 | A5 | A5 | A5 | A5 | A5 | ADDRESS INPUT |
| 124 | A4 | A4 | A4 | A4 | A4 | A4 | ADDRESS INPUT |
| 125 | VSS | VSS | VSS | VSS | VSS | VSS | PWR |
| 126 | VDD1 | VDD1 | VDD1 | VDD1 | VDD1 | VDD1 | PWR |
| 127 | A3 | A3 | A3 | A3 | A3 | A3 | ADDRESS INPUT |
| 128 | A2 | A2 | A2 | A2 | A2 | A2 | ADDRESS INPUT |
| 129 | A1 | A1 | A1 | A1 | A1 | A1 | ADDRESS INPUT |
| 130 | A0 | A0 | A0 | A0 | A0 | A0 | ADDRESS INPUT |
| 131 | VSS | VSS | VSS | VSS | VSS | VSS | PWR |
| 132 | VSS | VSS | VSS | VSS | VSS | VSS | PWR |

**Notes**:

NC Pins are not connected on the die

    1) BUSY# pin is an output for master devices only, and is a NC for slave devices.

    2) Control input when shown as En#, otherwise pin is NC.

    3) SCRUB# is an output for master devices, but an input for slave devices

## Master or Slave Options

To reduce the bit error rates, the SRAM devices employ an embedded EDAC (error detection and correction) with user programmable auto scrubbing options. The SRAM devices can automatically correct single bit word errors in event of an upset. During a read operation, if a multiple bit error occurs in a word, the SRAMs assert the MBE output to notify the host.

All SRAM devices are offered in two options: Master (UT8ER1M32M, UT8ER2M32M and UT8ER4M32M) or Slave (UT8ER1M32S, UT8ER2M32S and UT8ER4M32S). The masters are a full function device which features user defined autonomous EDAC scrubbing options. The slave device employs a scrub on demand feature.

The master and slave device pins $\overline{SCRUB}$ and $\overline{BUSY}$ are physically different. The $\overline{SCRUB}$ pin is an output on the master device, but an input on the slave device. The master $\overline{SCRUB}$ pin asserts low when a scrub cycle initiates, and can be used to demand scrub cycles from multiple slave units when connected to the $\overline{SCRUB}$ input of slave(s). The $\overline{BUSY}$ pin is an output for the master device and can be used to generate wait states by the memory controller. The $\overline{BUSY}$ pin is a no connect (NC) for slave devices.

## Device Operation

The SRAMs have control inputs called Chip Enable ($\overline{En}$), Write Enable ($\overline{W}$), and Output Enable ($\overline{G}$); 19 address inputs, A (18:0); and 32 bidirectional data lines, DQ (31:0). The $\overline{En}$ (chip enables) controls selection between active and standby modes. Asserting $\overline{En}$ enables the device, causes $I_{DD}$ to rise to its active value, and decodes the 19 address inputs. Only one chip enable may be active at any time. $\overline{W}$ controls read and write operations. During a read cycle, $\overline{G}$ must be asserted to enable the outputs.

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**Table 3. SRAM Device Control Operation Truth Table**

| $\overline{G}$ | $\overline{W}$ | $\overline{En}$ | I/O Mode | Mode |
|---|---|---|---|---|
| X | X | H | DQ (31:0)<br>3-State | Standby |
| L | H | L | DQ (31:0)<br>Data Out | Word Read |
| H | H | L | DQ (31:0)<br>All 3-State | Word Read[2] |
| X | L | L | DQ (31:0)<br>All 3-State | Word Write |

**Notes**:
1) "X" is defined as a "don't care" condition.
2) Device active; outputs disabled.

**Table 4. EDAC Control Pin Operation Truth Table**

| MBE | $\overline{SCRUB}$ | $\overline{BUSY}$ | I/O Mode | Mode |
|---|---|---|---|---|
| H | H | H | Read | Uncorrectable Multiple Bit Error |
| L | H | H | Read | Valid Data Out |
| X | H | H | X | Device Ready |
| X | H | L | X | Device Ready / Scrub Request Pending |
| X | L | X | Not Accessible | Device Busy |

**Notes**:
1) "X" is defined as a "don't care" condition.
2) $\overline{BUSY}$ signal is a "NC" for slave devices and are an "X" don't care.

## Read Cycle

A combination of $\overline{W}$ greater than $V_{IH}$ (min) with a single $\overline{En}$ and $\overline{G}$ less than $V_{IL}$ (max) defines a read cycle. Read access time is measured from the latter of device enable, output enable, or valid address to valid data output. Read cycles initiate with the assertion of any chip(s) enable or any address input change while any or all chip enables are asserted.

SRAM Read Cycle 1, the Address Access in Figure 3a, is initiated by a change in address inputs after a single $\overline{En}$ is asserted, $\overline{G}$ is asserted, $\overline{W}$ is deasserted and all are stable. Valid data appears on data outputs DQ(31:0) after the specified $t_{AVQV}$ is satisfied. Outputs remain active throughout the entire cycle. As long as device enable and output enable are active, the minimum time between valid address changes is specified by the read cycle time ($t_{AVAV}$). Changing addresses, prior to satisfying $t_{AVAV}$ minimum, results in an invalid operation. Invalid read cycles will require reinitialization.

SRAM Read Cycle 2, the Chip Enable-controlled Access in Figure 3b is initiated by a single $\overline{En}$ going active while $\overline{G}$ remains asserted, $\overline{W}$ remains deasserted, and the addresses remain stable for the entire cycle. After the specified $t_{ETQV}$ is satisfied, the 32-bit word addressed by A (18:0) is accessed and appears at the data outputs DQ(31:0).

SRAM Read Cycle 3, the Output Enable-controlled Access in Figure 3c, is initiated by $\overline{G}$ going active while a single $\overline{En}$ is asserted, $\overline{W}$ is deasserted, and the addresses are stable. Read access time is $t_{GLQV}$ unless $t_{AVQV}$ or $t_{ETQV}$ (reference Figure3b) have not been satisfied.

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SRAM EDAC Status Indications during a Read Cycle, if MBE is Low, the data is valid. If MBE is High, the data is corrupted (reference Table 3).

## Write Cycle

A combination of $\overline{W}$ and a single $\overline{En}$ less than $V_{IL}$(max) defines a write cycle. The state of $\overline{G}$ is a "don't care" for a write cycle. The outputs are placed in the high-impedance state when either $\overline{G}$ is greater than $V_{IH}$(min) or when $\overline{W}$ is less than $V_{IL}$(max).

Write Cycle 1, the Write Enable-controlled Access in Figure 4a, is defined by a write terminated by $\overline{W}$ going high with a single $\overline{En}$ still active. The write pulse width is defined by $t_{WLWH}$ when the write is initiated by $\overline{W}$ and by $t_{ETWH}$ when the write is initiated by $\overline{En}$. To avoid bus contention $t_{WLQZ}$ must be satisfied before data is applied to the 32 bidirectional pins DQ(31:0) unless the outputs have been previously placed in high impedance state by deasserting $\overline{G}$.

Write Cycle 2, the Chip Enable-controlled Access in Figure 4b, is defined by a write terminated by a single $\overline{En}$. The write pulse width is defined by $t_{WLEF}$ when the write is initiated by $\overline{W}$ and by $t_{ETEF}$ when the write is initiated by $\overline{En}$ going active. For the $\overline{W}$ initiated write, unless the outputs have been previously placed in the high-impedance state by $\overline{G}$, the user must wait $t_{WLQZ}$ before applying data to the 32 bidirectional pins DQ(31:0) to avoid bus contention.

## Control Register Write/Read Cycles

Configuration options can be selected by writing to the control register. The configuration tables (Tables 5 and 6) details the programming options. Scrub rate period and $\overline{BUSY}$ to $\overline{SCRUB}$ configurations are applicable to master devices using $\overline{E1}$ chip enables only. EDAC bypass and Read/Write control register is applicable to all valid chip enables $\overline{En}$. The control register is accessed by applying a series of values to the address bus as shown in Figures 7a and 7b. After the series the contents of the control register can be either read or written depending on the value of the corresponding read/write control register address pin (A(9) for odd die and A(2) for even die). **Note**: MBE must be driven high by the user for both a write or a read of the control register.

## Memory Scrubbing/Cycle Stealing

The SRAMs use architectural improvements and embedded error detection and correction to maintain unsurpassed levels of error protection. This is accomplished by what CAES refers to as Cycle Stealing. To minimize the system design impact on the speed of operation, the edge relationship between $\overline{BUSY}$ and $\overline{SCRUB}$ is programmable via the sequence described in figures 7a and 7b. The $\overline{BUSY}$ output is intended to give notification to the memory controller that a scrub cycle is impending. Since the memory cannot be accessed during an internal scrub cycle, the $\overline{BUSY}$ to SCRUB delay can be adjusted so the user may complete accesses prior to internal scrubbing.

The effective error rate is a function of the intrinsic error rate and the environment. Therefore, users are given the ability to control the scrub rate (ref. figure 7a) appropriate for the applicable environment. **Note:** the scrub rate will have an inverse relationship to the total throughput of the memory.

A master mode scrub cycle will occur at the user defined Scrub Rate Period. A scrub cycle is defined as the verification and correction (if necessary) of data for a single word address location. Address locations are scrubbed sequentially every Scrub Rate Period ($t_{SCRT}$). Scrub cycles will occur at every Scrub Rate Period regardless of the status of control pins. All inputs should remain stable while the $\overline{SCRUB}$ signal is active to avoid data corruption. Control pin function will be returned upon deassertion of $\overline{BUSY}$ pin.

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# UT8ER1M32, UT8ER2M32, UT8ER4M32

The Slave mode scrub cycle occurs anytime the $\overline{\text{SCRUB}}$ pin is asserted. The scrub cycle is defined the same as the master mode and will occur regardless of control pin status. Control pin function will be returned upon $\overline{\text{SCRUB}}$ deassertion.

Data is corrected during not only the internal scrub, but again during a user requested read cycle. If the data presented contains two or more errors after $t_{AVAV}$ is satisfied, the MBE signal will be asserted. (**Note:** Reading un-initialized memory locations may result in un-intended MBE assertions.)

### Table 5. Operational Environment [1]

| Total Dose | 100k | rads(Si) |
|---|---|---|
| Heavy Ion Error Rate[2] | $8.1 \times 10^{-16}$ | Errors/Bit-Day |

**Notes**:
1) The SRAM is immune to latchup to particles $\leq 110$MeV-cm$^2$/mg.
2) 90% worst case particle environment, Geosynchronous orbit, 100 mils of Aluminum and default EDAC scrub rate.

## Supply Sequencing

No supply voltage sequencing is required between $V_{DD1}$ and $V_{DD2}$

## Power-Up Requirements

During power-up of the SRAM devices, the power supply voltages will transverse through voltage ranges where the device is not guaranteed to operate before reaching final levels. Since some circuits on the device may operate at lower voltage levels than others, the device may power-up in an unknown state. To eliminate this with most power-up situations, the device employs an on-chip power-on-reset (POR) circuit. The POR, however, requires time to complete the operation. Therefore, it is recommended that all device activity be delayed by a minimum of 100ms, after both $V_{DD1}$ and $V_{DD2}$ supplies have reached stable minimum operating voltage.

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# UT8ER1M32, UT8ER2M32, UT8ER4M32

## Absolute Maximum Ratings[1]

(Referenced to $V_{SS}$)

| Symbol | Parameter | Limits |
|---|---|---|
| $V_{DD1}$ | DC supply voltage (Core) | -0.3 to 2.4V |
| $V_{DD2}$ | DC supply voltage (I/O) | -0.3 to 4.5V |
| $V_{I/O}$ | Voltage on any pin | -0.3 to 4.5V |
| $T_{STG}$ | Storage temperature | -65 to +150°C |
| $P_D$[2]: <br> UT8ER1M32 <br> UT8ER2M32 <br> UT8ER4M32 | Maximum package power dissipation permitted @ $T_C$= +105°C | 3.3W <br> 2W <br> 1.3W |
| $T_J$ | Maximum junction temperature | +150°C |
| $\Theta_{JC}$[3]: <br> UT8ER1M32 <br> UT8ER2M32 <br> UT8ER4M32 | Thermal resistance, junction-to-case[2] | 6°C/W <br> 10°C/W <br> 15°C/W |
| $I_I$ | DC input current | ±10 mA |

**Notes**:

1) Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition beyond limits indicated in the operational sections of this specification is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability and performance.

2) Per MIL-STD-883, Method 1012, Section 3.4.1, $\dfrac{P_D=(125°C - 105°C)}{\Theta_{JC}}$

3) $\Theta_{JC}$ varies with density due to stacked die configuration.

## Recommended Operating Conditions

| Symbol | Parameter | Limits |
|---|---|---|
| $V_{DD1}$ | DC supply voltage (Core) | 1.7 to 2.0V |
| $V_{DD2}$ | DC supply voltage (I/O) | 2.3 to 3.6V |
| $T_C$ | Case temperature range | -55 to +105°C |
| $V_{IN}$ | DC input voltage | 0V to $V_{DD2}$ |

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# UT8ER1M32, UT8ER2M32, UT8ER4M32

## DC Electrical Characteristics (Pre and Post-Radiation)*

($V_{DD1}$ = 1.7V to 2.0V, $V_{DD2}$ = 2.3V to 3.6V; Unless otherwise noted, Tc is per the temperature range ordered)

| Symbol | Parameter | Condition | | MIN | MAX | Unit |
|---|---|---|---|---|---|---|
| $V_{IH1}$ | High-level input voltage | VDD1 = 2.0V, VDD2 = 3.6V<br>VDD1 = 1.7V, VDD2 = 3.0V | | 2.2 | | V |
| $V_{IL1}$ | Low-level input voltage | VDD1 = 2.0V, VDD2 = 3.6V<br>VDD1 = 1.7V, VDD2 = 3.0V | | | 0.8 | V |
| $V_{IH2}$ | High-level input voltage | VDD1 = 2.0V, VDD2 = 2.7V | | 1.6 | | |
| $V_{IL2}$ | Low-level input voltage | VDD1 = 1.7V, VDD2 = 2.3V | | | 0.7 | V |
| $V_{OL1}$[1] | Low-level output voltage | $I_{OL}$ = 8mA, $3.0V \leq V_{DD2} \leq 3.6V$ | | | 0.4 | V |
| $V_{OL2}$[1] | Low-level output voltage | $I_{OL}$ = 6mA, $2.3V \leq V_{DD2} \leq 2.7V$ | | | $0.2*V_{DD2}$ | V |
| $V_{OH1}$ | High-level output voltage | $I_{OH}$ = -4mA, $3.0V \leq V_{DD2} \leq 3.6V$ | | $0.8*V_{DD2}$ | | V |
| $V_{OH2}$ | High-level output voltage | $I_{OL}$ = -2mA, $2.3V \leq V_{DD2} \leq 2.7V$ | | $0.8*V_{DD2}$ | | V |
| $I_{IN}$ | Input leakage current | $V_{IN}$ = $V_{DD2}$ and $V_{SS}$ | | -2 | 2 | µA |
| $I_{OZ}$[3] | Three-state output leakage current | $V_O$ = $V_{DD2}$ and $V_{SS}$<br>$V_{DD2}$ = $V_{DD2}$ (max), $\overline{G}$ = $V_{DD2}$ (max) | | -2 | 2 | µA |
| $I_{OS}$[4,5] | Short-circuit output current | $V_{DD2}$ = $V_{DD2}$ (max), $V_O$ = $V_{DD2}$<br>$V_{DD2}$ = $V_{DD2}$ (max), $V_O$ = $V_{SS}$ | | -100 | +100 | mA |
| $I_{DD1}(OP_1$[6,8]$)$ | $V_{DD1}$ Supply current read operation @ 1MHz, EDAC enabled @ default Scrub Rate Period (see table 5). | Inputs: $V_{IL}$ = $V_{SS}$ + 0.2V, $V_{IH}$ = $V_{DD2}$ -0.2V, $I_{OUT}$ = 0 $V_{DD1}$ = $V_{DD1}$ (max), $V_{DD2}$ = $V_{DD2}$ (max) | $V_{DD1}$ = 2.0V | | 14 | mA |
| | | | $V_{DD1}$ = 1.9V | | 10 | mA |
| $I_{DD1}(OP_2$[6,8,9]$)$ | $V_{DD1}$ Supply current read operation @ fmax, EDAC enabled @ default Scrub Rate Period (see table 5). | Inputs: $V_{IL}$ = $V_{SS}$ + 0.2V, $V_{IH}$ = $V_{DD2}$ -0.2V, $I_{OUT}$ = 0 $V_{DD1}$ = $V_{DD1}$ (max), $V_{DD2}$ = $V_{DD2}$ (max) | $V_{DD1}$ = 2.0V<br>$V_{DD1}$ = 1.9V<br>UT8ER4M32 | | 230<br>215 | mA<br>mA |
| | | | $V_{DD1}$ = 2.0V<br>$V_{DD1}$ = 1.9V<br>UT8ER1M32<br>UT8ER2M32 | | 225<br>210 | mA<br>mA |
| $I_{DD2}(OP_1$[6,8]$)$ | $V_{DD2}$ Supply current read operation @ 1MHz, EDAC enabled @ default Scrub Rate Period (see table 5). | Inputs: $V_{IL}$ = $V_{SS}$ + 0.2V, $V_{IH}$ = $V_{DD2}$ -0.2V, $I_{OUT}$ = 0 $V_{DD1}$ = $V_{DD1}$ (max), $V_{DD2}$ = $V_{DD2}$ (max) | | | 2 | mA |
| $I_{DD2}(OP_2$[6,8,9]$)$ | $V_{DD2}$ Supply current read operation @ fmax, EDAC enabled @ default Scrub Rate Period (see table 5). | Inputs: $V_{IL}$ = $V_{SS}$ + 0.2V, $V_{IH}$ = $V_{DD2}$ -0.2V, $I_{OUT}$ = 0 $V_{DD1}$ = $V_{DD1}$ (max), $V_{DD2}$ = $V_{DD2}$ (max) | | | 5 | mA |

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# UT8ER1M32, UT8ER2M32, UT8ER4M32

| Symbol | Parameter | Condition | | MIN | MAX | Unit |
|---|---|---|---|---|---|---|
| $I_{DD1}(SB)^{7,10}$ | Supply current standby @ 0Hz, EDAC disabled (per die) | CMOS inputs, $I_{OUT} = 0$ $\overline{En} = V_{DD2}$ -0.2 $V_{DD1} = V_{DD1}$ (max), $V_{DD2} = V_{DD2}$ (max) | -55°C and 25°C | | 15 | mA |
| | | | 105°C | | 35 | mA |
| $I_{DD2}(SB)^{10}$ | Supply current standby @ 0Hz, EDAC disabled (per die) | CMOS inputs, $I_{OUT} = 0$ $\overline{En} = V_{DD2}$ -0.2 $V_{DD1} = V_{DD1}$ (max), $V_{DD2} = V_{DD2}$ (max) | | | 3 | mA |
| $I_{DD1}(SB)^{7,9,10}$ | Supply current standby A (16:0) @ fmax, EDAC disabled (per die) | CMOS inputs, $I_{OUT} = 0$ $\overline{En} = V_{DD2}$ - 0.2 $V_{DD1} = V_{DD1}$ (max), $V_{DD2} = V_{DD2}$ (max) | -55°C and 25°C | | 15 | mA |
| | | | 105°C | | 35 | mA |
| $I_{DD2}(SB)^{9,10}$ | Supply current standby A (16:0) @ fmax, EDAC disabled (per die) | CMOS inputs, $I_{OUT} = 0$ $\overline{En} = V_{DD2}$ - 0.2 $V_{DD1} = V_{DD1}$ (max), $V_{DD2} = V_{DD2}$ (max) | | | 3 | mA |

## Capacitance

| Symbol | Parameter | Condition | UT8ER1M32 | | UT8ER2M32 | | UT8ER4M32 | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $C_{IN}^2$ | Input capacitance | $f$ = 1MHz @ 0V | | 18 | | 29 | | 50 | pF |
| $C_{En}^2$ | Input capacitance Device Enables | $f$ = 1MHz @ 0V | | 10 | | 10 | | 10 | pF |
| $C_{IO}^2$ | Bidirectional I/O capacitance | $f$= 1MHz @ 0V | | 15 | | 27 | | 50 | pF |

**Notes**:
* For devices procured with a total ionizing dose tolerance guarantee, the post-irradiation performance is guaranteed at 25°C per MIL-STD-883 Method 1019, Condition A up to the maximum TID level procured.

1) The $\overline{SCRUB}$ and $\overline{BUSY}$ pins for UT8ER1M32M, UT8ER2M32M and UT8ER4M32M (master) are tested functionally for VOL specification.
2) Measured only for initial qualification and after process or design changes that could affect this parameter.
3) The $\overline{SCRUB}$ and $\overline{BUSY}$ pins for UT8ER1M32M, UT8ER2M32M and UT8ER4M32M (master) are guaranteed by design, but neither tested nor characterized.
4) Supplied as a design limit but not guaranteed or tested.
5) Not more than one output may be shorted at a time for maximum duration of one second.
6) EDAC enabled. Default Scrub Rate Period applicable to master device only.
7) Post radiation limits are the 105°C temperature limit when specified.
8) Operating current limit does not include standby current.
9) fmax = 50MHz
10) $V_{IH} = V_{DD2}$ (max), $V_{IL} = 0V$

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# UT8ER1M32, UT8ER2M32, UT8ER4M32

## AC Characteristics Read Cycle (Pre and Post-Radiation)[*]

($V_{DD1}$ = 1.7V to 2.0V, $V_{DD2}$ = 2.3V to 3.6V); Unless otherwise noted, Tc is per the temperature range ordered

| Symbol | Parameter | UT8ER1M32 | | UT8ER2M32 | | UT8ER4M32 | | Unit | Figure |
|---|---|---|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | MIN | MAX | | |
| $t_{AVAV1}$[1,4] | Read cycle time | 20 | | 22 | | 25 | | ns | 3a |
| $t_{AVSK}$[3] | Address valid to address valid skew line | | 4 | | 4 | | 4 | ns | 3a |
| $t_{AVQV}$[1] | Address to data valid from address change | | 20 | | 22 | | 25 | ns | 3c |
| $t_{AXQX}$[2] | Output hold time | 1.5 | | 1.5 | | 1.5 | | ns | 3a |
| $t_{GLQX}$[1,2] | $\overline{G}$-controlled output enable time | 1 | | 1 | | 1 | | ns | 3c |
| $t_{GLQV}$ | $\overline{G}$-controlled output data valid | | 10 | | 10 | | 10 | ns | 3c |
| $t_{GHQZ1}$[2] | $\overline{G}$-controlled output three-state time | 1 | 8 | 1 | 8 | 1 | 8 | ns | 3c |
| $t_{ETQX}$[2] | E-controlled output enable time | 4 | | 4 | | 4 | | ns | 3b |
| $t_{ETQV}$ | E-controlled access time | | 20 | | 22 | | 25 | ns | 3b |
| $t_{AVET2}$[3] | Address setup time for read (E-controlled) | -4 | | -4 | | -4 | | ns | 3b |
| $t_{EFQZ}$[2] | E-controlled output three-state time[2] | 2 | 9 | 2 | 9 | 2 | 9 | ns | 3b |
| $t_{AVMV}$ | Address to error flag valid | | 22 | | 22 | | 22 | ns | 3a |
| $t_{AXMX}$[2] | Address to error flag hold time from address change | 1.5 | | 1.5 | | 1.5 | | ns | 3a |
| $t_{GLMX}$[2] | $\overline{G}$-controlled error flag enable time | 0 | | 0 | | 0 | | ns | 3c |
| $t_{GLMV}$ | $\overline{G}$-controlled error flag valid | | 8 | | 8 | | 8 | ns | |
| $t_{ETMX}$[2] | E-controlled error flag enable time | 4 | | 4 | | 4 | | ns | 3b |
| $t_{ETMV}$ | E-controlled error flag time | | 22 | | 22 | | 25 | ns | 3b |
| $t_{GHMZ}$[2] | G-controlled error flag three-state time | 1 | 9 | 1 | 9 | 1 | 9 | ns | 3b |

**Notes**:
* For devices procured with a total ionizing dose tolerance guarantee, the post-irradiation performance is guaranteed at 25°C per MIL-STD-883 Method 1019, Condition A up to the maximum TID level procured.
1) Guaranteed by characterization, but not tested.
2) Three-state is defined as a change from steady-state output voltage.
3) Guaranteed by design.
4) Address changes prior to satisfying $t_{AVAV}$ minimum is an invalid operation.

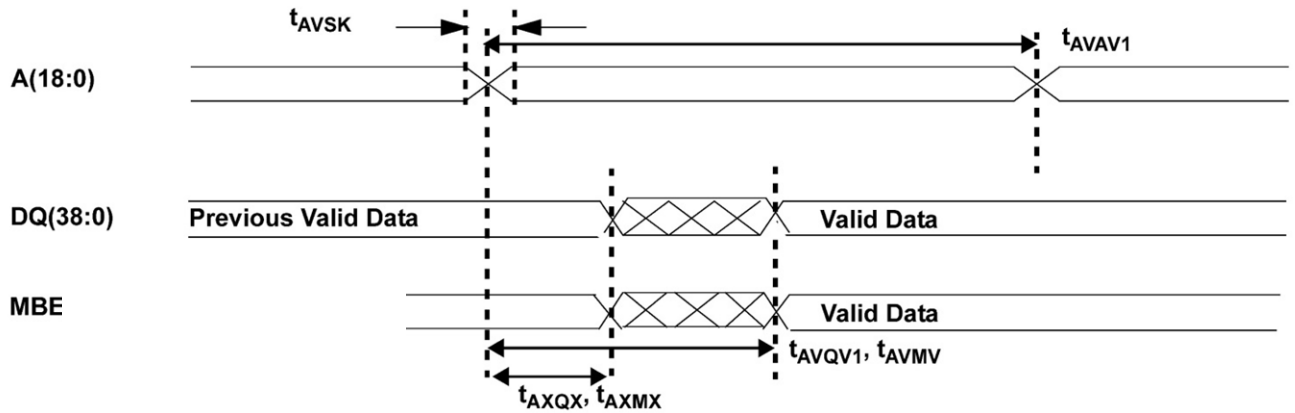32, 64, 128 Megabit SRAM MCM

# UT8ER1M32, UT8ER2M32, UT8ER4M32



Figure 3a. SRAM Read Cycle 1: Address Access

**Assumptions:**

1) $\overline{En}$ and $\overline{G} \leq V_{IL}$ (max) and $\overline{W} \geq V_{IH}$ (min)

2) $\overline{SCRUB} \geq V_{OH}$ (min)

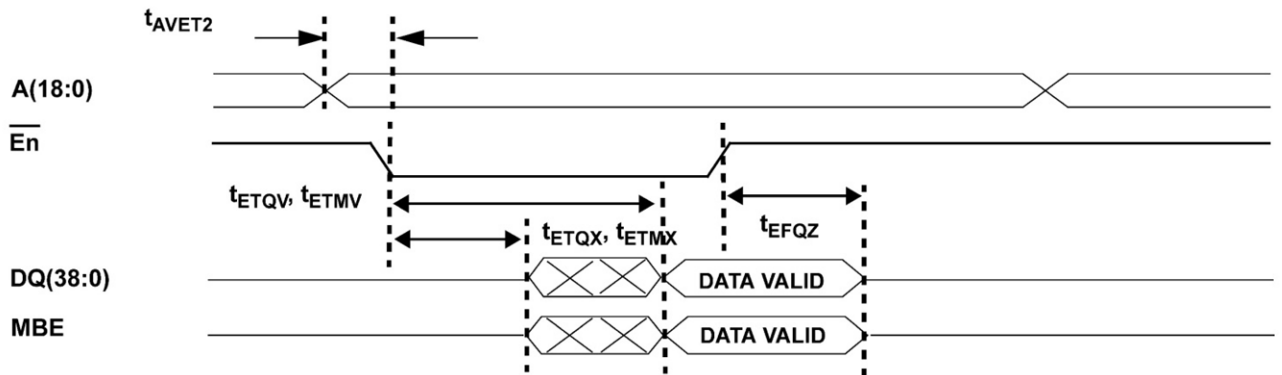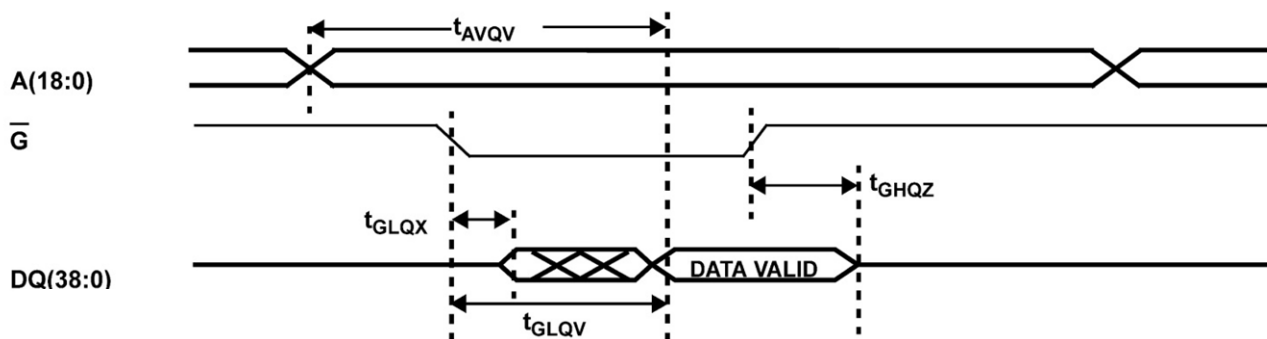3) Reading uninitialized address may cause MBE to be asserted.



Figure 3b. SRAM Read Cycle 2: Chip Enable Access

**Assumptions:**

1) $\overline{G} \leq V_{IL}$ (max) and $\overline{W} \geq V_{IH}$ (min)

2) $\overline{SCRUB} \geq V_{OH}$ (min)

3) Reading uninitialized address may cause MBE to be asserted.

# UT8ER1M32, UT8ER2M32, UT8ER4M32



Figure 3c. SRAM Read Cycle 3: Output Enable Access

**Assumptions:**

1) $\overline{E} \le V_{IL}$ (max) and $\overline{W} \ge V_{IH}$ (min)

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# UT8ER1M32, UT8ER2M32, UT8ER4M32

**AC Electrical Characteristics Write Cycle (Pre and Post-Radiation)***

($V_{DD1}$ = 1.7V to 2.0V, $V_{DD2}$ = 2.3V to 3.6V); Unless otherwise noted, Tc is per the temperature range ordered

| Symbol | Parameter | UT8ER1M32 | | UT8ER1M32 | | UT8ER1M32 | | Unit | Figure |
|---|---|---|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | MIN | MAX | | |
| $t_{AVAV2}$[1] | Write cycle time | 10 | | 10 | | 10 | | ns | 4a/4b |
| $t_{ETWH}$ | Device enable to end of write | 10 | | 10 | | 10 | | ns | 4a |
| $t_{AVET}$ | Address setup time for write ($\overline{En}$- controlled) | 0 | | 0 | | 0 | | ns | 4b |
| $t_{AVWL}$ | Address setup time for write ($\overline{W}$ - controlled) | 0 | | 0 | | 0 | | ns | 4a |
| $t_{WLWH}$[1] | Write pulse width | 8 | | 8 | | 8 | | ns | 4a |
| $t_{WHAX}$ | Address hold time for write ($\overline{W}$ - controlled) | 0 | | 0 | | 0 | | ns | 4a |
| $t_{EFAX}$ | Address hold time for device enable ($\overline{En}$ - controlled) | 0 | | 0 | | 0 | | ns | 4b |
| $t_{WLQZ}$[2] | $\overline{W}$ - controlled three-state time | | 9 | | 9 | | 9 | ns | 4a/4b |
| $t_{WHQX}$[2] | $\overline{W}$ - controlled output enable time | 0 | | 0 | | 0 | | ns | 4a |
| $t_{ETEF}$ | Device enable pulse width ($\overline{En}$ - controlled) | 10 | | 10 | | 10 | | ns | 4b |
| $t_{DVWH}$ | Data setup time | 5 | | 5 | | 6 | | ns | 4a |
| $t_{WHDX}$ | Data hold time | 0 | | 0 | | 0 | | ns | 4a |
| $t_{WLEF}$[1] | Device enable controlled write pulse width | 8 | | 8 | | 8 | | ns | 4b |
| $t_{DVEF}$ | Data setup time | 5 | | 5 | | 6 | | ns | 4a/4b |
| $t_{EFDX}$ | Data hold time | 0 | | 0 | | 0 | | ns | 4b |
| $t_{AVWH}$ | Address valid to end of write | 10 | | 10 | | 10 | | ns | 4a |
| $t_{WHWL}$[1] | Write disable time | 2 | | 2 | | 3 | | ns | 4a |

**Notes**:

* For devices procured with a total ionizing dose tolerance guarantee, the post-irradiation performance is guaranteed at 25°C per MIL-STD-883 Method 1019, Condition A up to the maximum TID level procured.

1) Tested with $\overline{G}$ high.
2) Three-state is defined as a change from steady-state output voltage.

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# UT8ER1M32, UT8ER2M32, UT8ER4M32
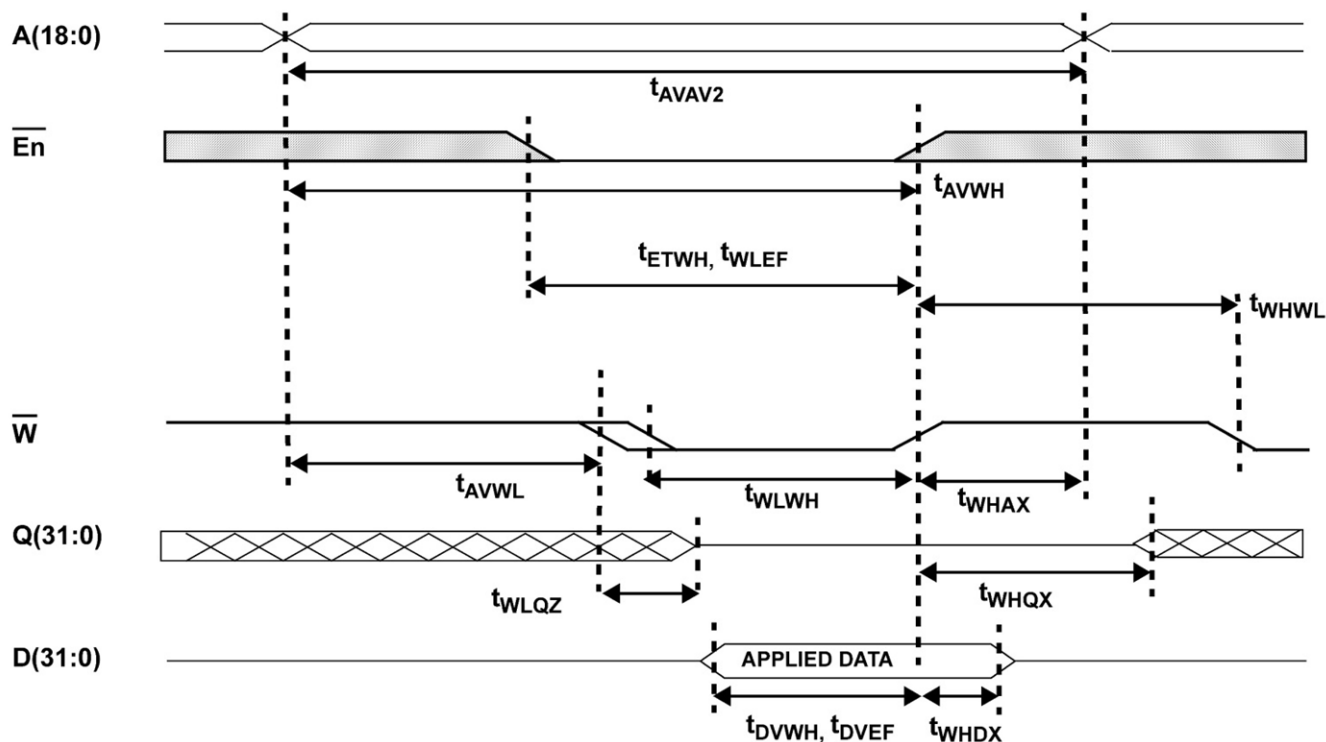


Figure 4a. SRAM Write Cycle 1: $\overline{W}$ - Controlled Access

**Assumptions:**

1) $\overline{G} \le V_{IL}$ (max). (If $\overline{G} \ge V_{IH}$ (min) then Q(31:0) and MBE will be in the three-state for the entire cycle.)

2) $\overline{SCRUB} \ge V_{OH}$ (min)
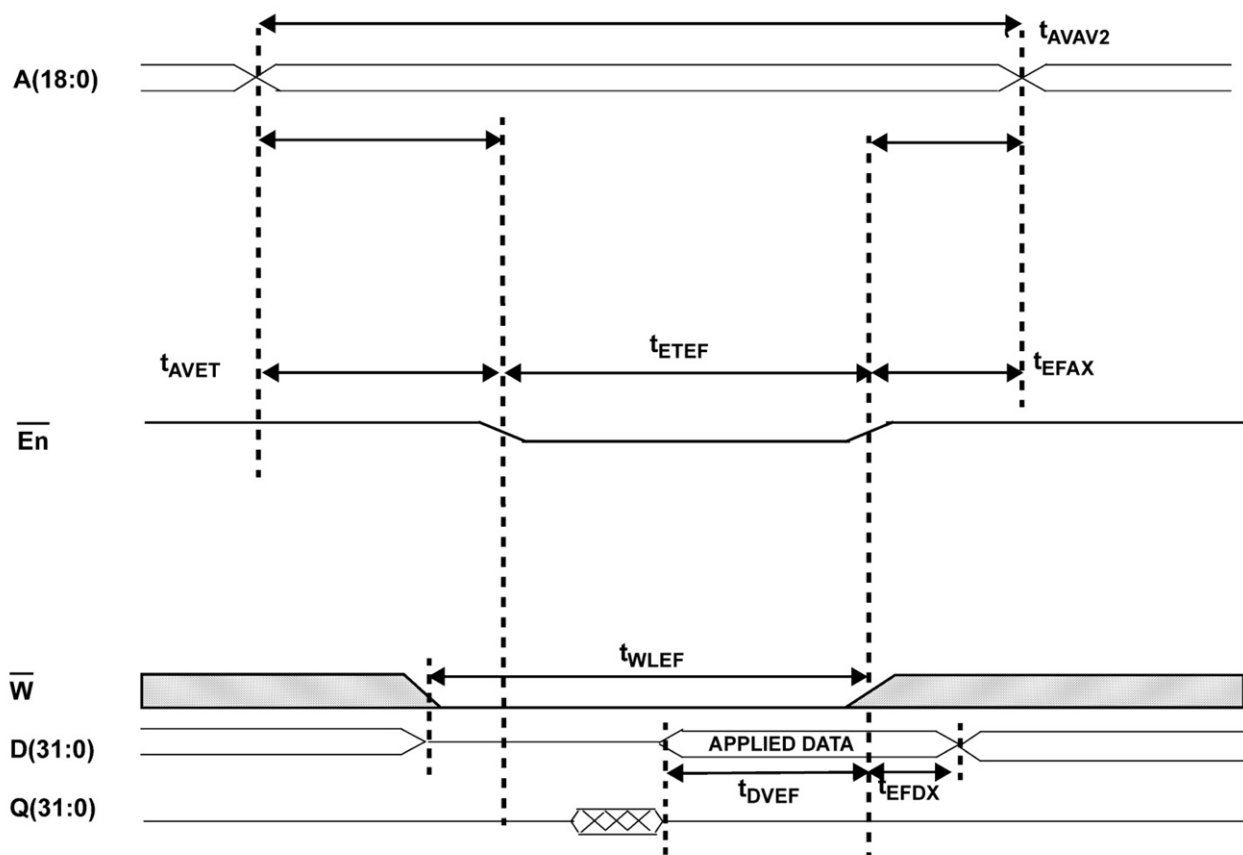
Figure 4b. SRAM Write Cycle 2: Enable - Controlled Access
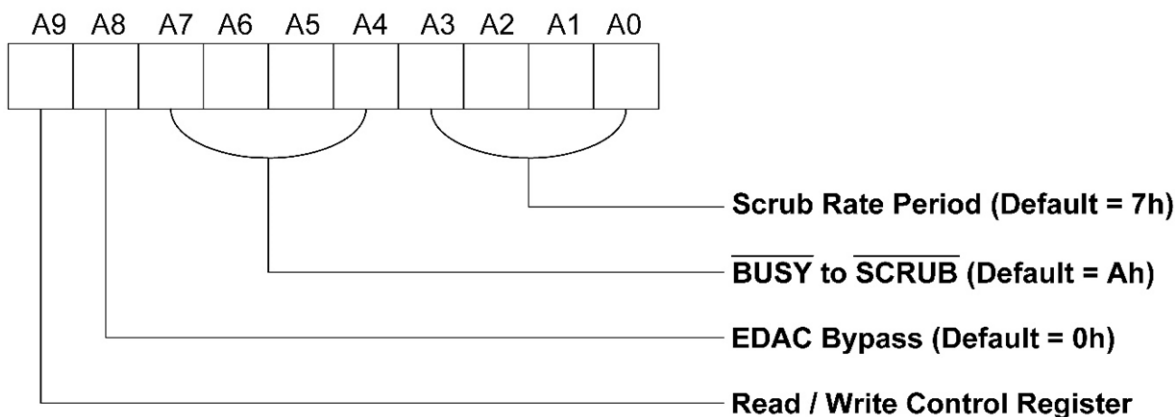
**Assumptions:**

1) $\overline{G} \le V_{IL}$ (max). (If $\overline{G} \ge V_{IH}$ (min) then Q(31:0) and MBE will be in the three-state for the entire cycle. )

2) $\overline{Busy} \ge V_{OH}$ (min)



**Scrub Rate Period (Default = 7h)**

$\overline{BUSY}$ to $\overline{SCRUB}$ (Default = Ah)

**EDAC Bypass (Default = 0h)**

**Read / Write Control Register**

Figure 5. (Odd Die Numbers ($\overline{E1}$, $\overline{E3}$, $\overline{E5}$, $\overline{E7}$ Chip Enables) EDAC Control Register

**Note**:

1)   See Table 5 for Control Register Definitions

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# UT8ER1M32, UT8ER2M32, UT8ER4M32

**Table 6: (Odd Die Numbers (E1, E3, E5, E7 Chip Enables) EDAC Programming Configuration Table**

| ADDR Bit | Parameter | Value | Function |
|---|---|---|---|
| A (3-0) | Scrub Rate Period[1,2,3] | 3-15<br>Note:<br>0-2<br>reserved | As Scrub Rate Period changes from 0 - 15, then the interval between Scrub cycles will change as follows:<br>3 = 600 ns     8 = 13.0 us     12 = 205 us<br>4 = 1000 ns    9 = 25.8 us     13 = 409.8 us[4]<br>5 = 1800 ns    10 = 51.4 us    14 = 819.4 us[4]<br>6 = 3400 ns    11 = 102.6 us   15 = 1.64 ms[4]<br>7 = 6600 ns |
| A (7-4) | $\overline{BUSY}$ to $\overline{SCRUB}$[1,3,5] | 0-15 | If $\overline{BUSY}$ to $\overline{SCRUB}$ changes from 0 - 15, then the interval $t_{BLSL}$ between $\overline{SCRUB}$ and BUSY will change as follows:<br>0 = 0 ns      6 = 300 ns     11 = 550 ns<br>1 = 50 ns     7 = 350 ns     12 = 600 ns<br>2 = 100 ns    8 = 400 ns     13 = 650 ns<br>3 = 150 ns    9 = 450 ns     14 = 700 ns<br>4 = 200 ns    10 = 500 ns    15 = 750 ns<br>5 = 250ns |
| A (8) | Bypass EDAC Bit[6,7] | 0, 1 | If 0, then normal EDAC operation will occur.<br>If 1, then EDAC will be bypassed and no memory scrubbing will occur. |
| A (9) | Read / $\overline{Write}$ Control Register | 0, 1 | 0 = A8 to A0 will be written to the control register.<br>1 = Control register will be asserted to the data bus DQ[8:0] respectively. |

**Notes**:
1) Values based on minimum specifications. For guaranteed ranges of Scrub Rate Period ($t_{SCRT}$) and $\overline{BUSY}$ to $\overline{SCRUB}$ ($t_{BLSL}$), reference the Master Mode AC Characteristic.
2) Default Scrub Rate Period is 6600 ns.
3) Scrub Rate Period and $\overline{BUSY}$ to $\overline{SCRUB}$ applicable to the master devices die #1 ($\overline{E1}$ chip enable) only.
4) Period below test capability.
5) The default for $t_{BLSL}$ is 500 ns.
6) The default state for A8 is 0.
7) The EDAC bypass option is provided for memory accesses when error correction is not desired (i.e. device and system testing).
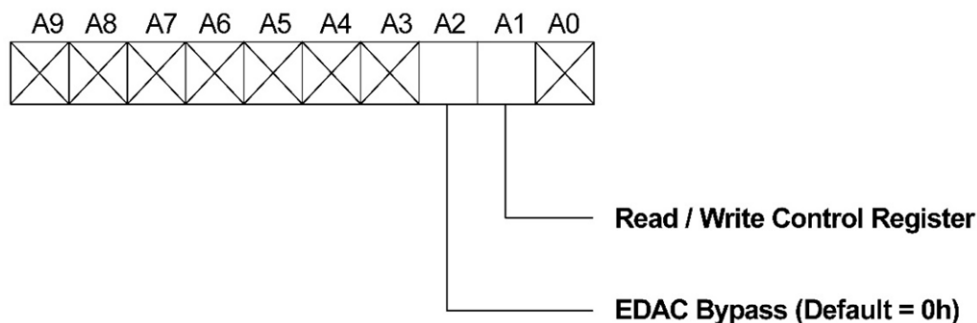


Figure 6. (Even Die Numbers ($\overline{E2}$, $\overline{E4}$, $\overline{E6}$, $\overline{E8}$ Chip Enables) EDAC Control Register

**Note**:
X = Not applicable for even die.
1) See Table 6 for Control Register Definitions

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# UT8ER1M32, UT8ER2M32, UT8ER4M32

**Table 7: Even Die Numbers ($\overline{E2}$, $\overline{E4}$, $\overline{E6}$, $\overline{E8}$ Chip Enables) EDAC Programming Configuration Table**

| ADDR Bit | Parameter | Value | Function |
|---|---|---|---|
| A (2) | Bypass EDAC Bit[1,2] | 0, 1 | If 0, then normal EDAC operation will occur.<br>If 1, then EDAC will be bypassed and no memory scrubbing will occur. |
| A (1) | Read / $\overline{\text{Write}}$ Control Register | 0, 1 | 0 = A2 will be written to the control register<br>1 = Control register will be asserted to the data bus DQ18 |

**Notes**:
1) The default state for A2 is 0.
2) The EDAC bypass option is provided for memory accesses when error correction is not desired (i.e. device and system testing).

## EDAC Control Register AC Characteristics (Pre and Post-Radiation)*

($V_{DD1}$ = 1.7V to 2.0V, $V_{DD2}$ = 2.3V to 3.6V); Unless otherwise noted, Tc is per the temperature range ordered

| Symbol | Parameter | UT8ER1M32<br>UT8ER2M32<br>UT8ER4M32 | | Unit | Figure |
|---|---|---|---|---|---|
| | | MIN | MAX | | |
| $t_{AVAV3}$ | Address valid to address valid for control register cycle | 200 | | ns | 7a, 7b |
| $t_{AVCL}$ | Address valid to control low | 400 | | ns | 7a, 7b |
| $t_{AVEX}$ | Address valid to enable de-assertion | 200 | | ns | 7a, 7b |
| $t_{AVQV3}$ | Address to data valid control register read | | 400 | ns | 7a, 7b |
| $t_{MLQX}$[1] | MBE control EDAC disable time | 3 | | ns | 7a, 7b |
| $t_{CHAV}$ | MBE high to address valid | 0 | | ns | 7a, 7b |
| $t_{CLAX}$ | MBE low to address invalid | 0 | | ns | 7a, 7b |
| $t_{GHQZ3}$[1] | Output tri-state time | 2 | 9 | ns | 7a, 7b |
| $t_{MLGL}$[2] | MBE low to output enable | 85 | | ns | 7a, 7b |

**Notes**:
\* For devices procured with a total ionizing dose tolerance guarantee, the post-irradiation performance is guaranteed at 25°C per MIL-STD-883 Method 1019, Condition A up to the maximum TID level procured.
1) Three-state is defined as a change from steady-state output.
2) Guaranteed by design neither tested or characterized.
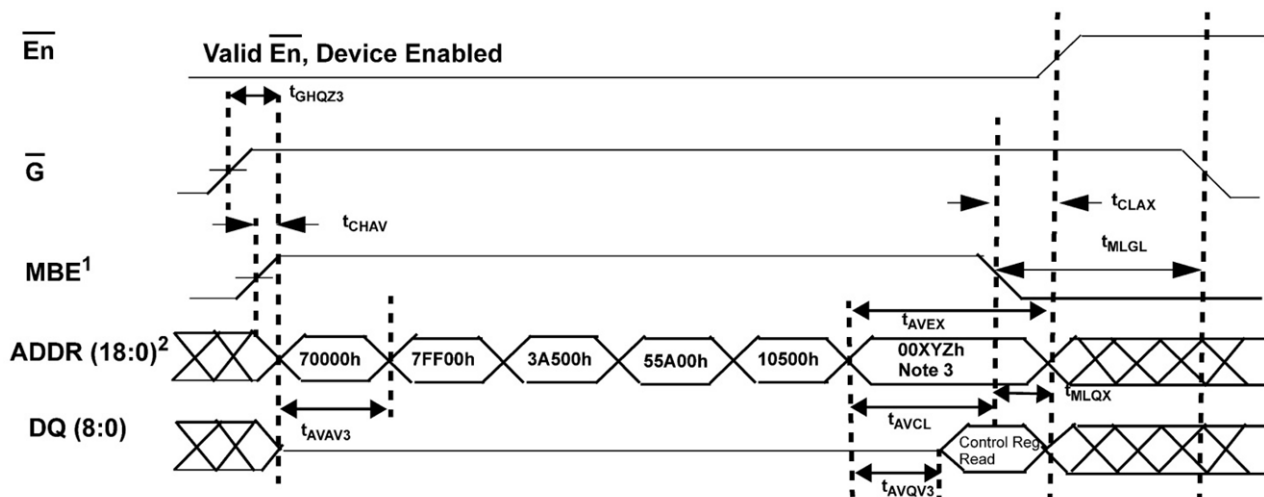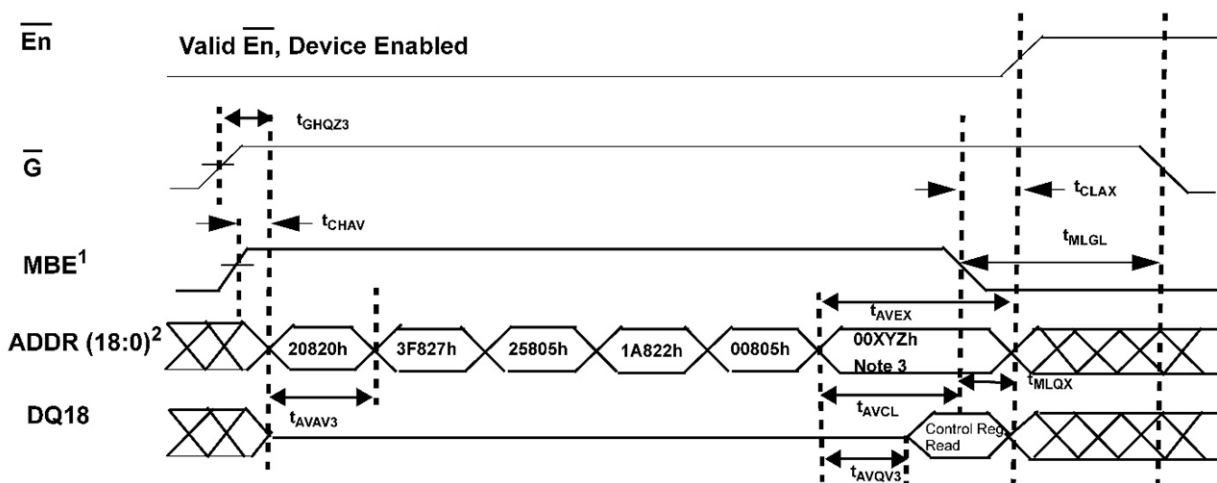
# UT8ER1M32, UT8ER2M32, UT8ER4M32



Figure 7a. Odd Die Numbers ($\overline{E1}$, $\overline{E3}$, $\overline{E5}$, $\overline{E7}$ Chip Enables) EDAC Control Register Cycle

**Note**s:
1) MBE is driven high by the user.
2) Device must see a transition to address 70000h coincident with or subsequent to MBE assertion
3) Lower 10 bits of the last address are used to read or configure the control register (ref Control Register Write/Read Cycles page 11 and Table 5).

**Assumptions:**
1) $\overline{SCRUB} \geq V_{OH}$ before the start of the configuration cycle. Ignore $\overline{SCRUB}$ during configuration cycle.



Figure 7b. Even Die Numbers ($\overline{E2}$, $\overline{E4}$, $\overline{E6}$, $\overline{E8}$ Chip Enables) EDAC Control Register Cycle

**Notes**:
1) MBE is driven high by the user.
2) Device must see a transition to address 20820h coincident with or subsequent to MBD assertion.
3) Bits A2 and A1 are used to read or configure the control register (ref Control Register Write/Read Cycles page 20 and Table 6)

**Assumptions:**
1) $\overline{SCRUB} \geq V_{OH}$ before the start of the configuration cycle. Ignore $\overline{SCRUB}$ during configuration cycle.

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# UT8ER1M32, UT8ER2M32, UT8ER4M32

## Master Mode AC Characteristics (Pre and Post-Radiation) *

$V_{DD1}$ = 1.7V to 2.0V, $V_{DD2}$ = 2.3V to 3.6V); Unless otherwise noted, Tc is per the temperature range ordered

| Symbol | Parameter | MIN | MAX | Unit | Figure |
|--------|-----------|-----|-----|------|--------|
| $t_{BLSL}$[1] | User Programmable - $\overline{BUSY}$ low to $\overline{SCRUB}$ | 50*n | (90*n)+1 | ns | 7c |
| $t_{SLSH1}$ | $\overline{SCRUB}$ low to $\overline{SCRUB}$ high | 200 | 350 | ns | 7c |
| $t_{SHBH}$ | $\overline{SCRUB}$ high to $\overline{BUSY}$ high | 50 | 85 | ns | 7c |
| $t_{SCRT}$[2] | Scrub Rate Period | $2^n*50+200$ | $2^n*90+350$ | ns | 7c |

**Notes**:

* For devices procured with a total ionizing dose tolerance guarantee, the post-irradiation performance is guaranteed at 25°C per MIL-STD-883 Method 1019, Condition A up to the maximum TID level procured.

    1) See Table 5 for User Programmable information. The value "n" is decimal equivalent of hexadecimal value 0x0 through 0xF programmed into control register address bits $A_4$-$A_7$ by user. Default value "n" = 10.

    2) See Table 5 for User Programmable information. The value "n" is decimal equivalent of hexadecimal value 0x3 through 0xF programmed into control register address bits $A_0$-$A_3$. Default value is "n" = 7.
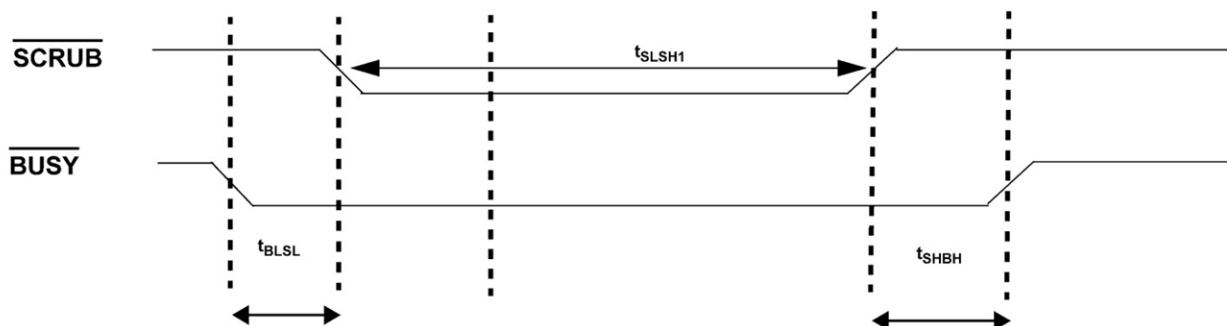


Figure 7c. Master Mode Scrub Cycle

**Assumptions:**

    1) The conditions pertain to both a Read or Write.

## Slave Mode AC Characteristics (Pre and Post-Radiation)*

$V_{DD1}$ = 1.7V to 1.9V, $V_{DD2}$ = 2.3V to 3.6V) Unless otherwise noted, Tc is per the temperature range ordered

| Symbol | Parameter | MIN | MAX | Unit | Figure |
|--------|-----------|-----|-----|------|--------|
| $t_{SLSH2}$ | $\overline{SCRUB}$ low to $\overline{SCRUB}$ high (slave) | 200 | | ns | 7d |
| $t_{SHSL}$[1] | $\overline{SCRUB}$ high to $\overline{SCRUB}$ low (slave) | 400 | | ns | 7d |

**Note**:

* For devices procured with a total ionizing dose tolerance guarantee, the post-irradiation performance is guaranteed at 25°C per MIL-STD-883 Method 1019, Condition A up to the maximum TID level procured.

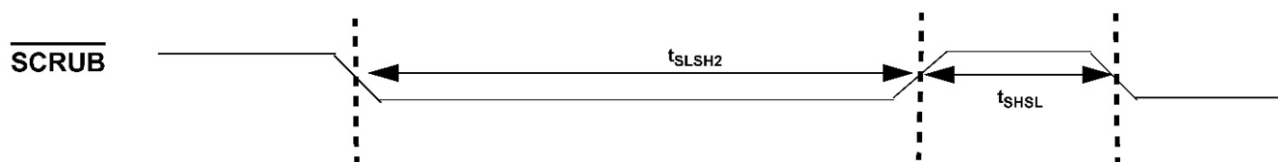    1) Guaranteed by design, neither tested nor characterized.



Figure 7d. Slave Mode Scrub Cycle

**Assumptions:**

    1) The conditions pertain to both a Read or Write.
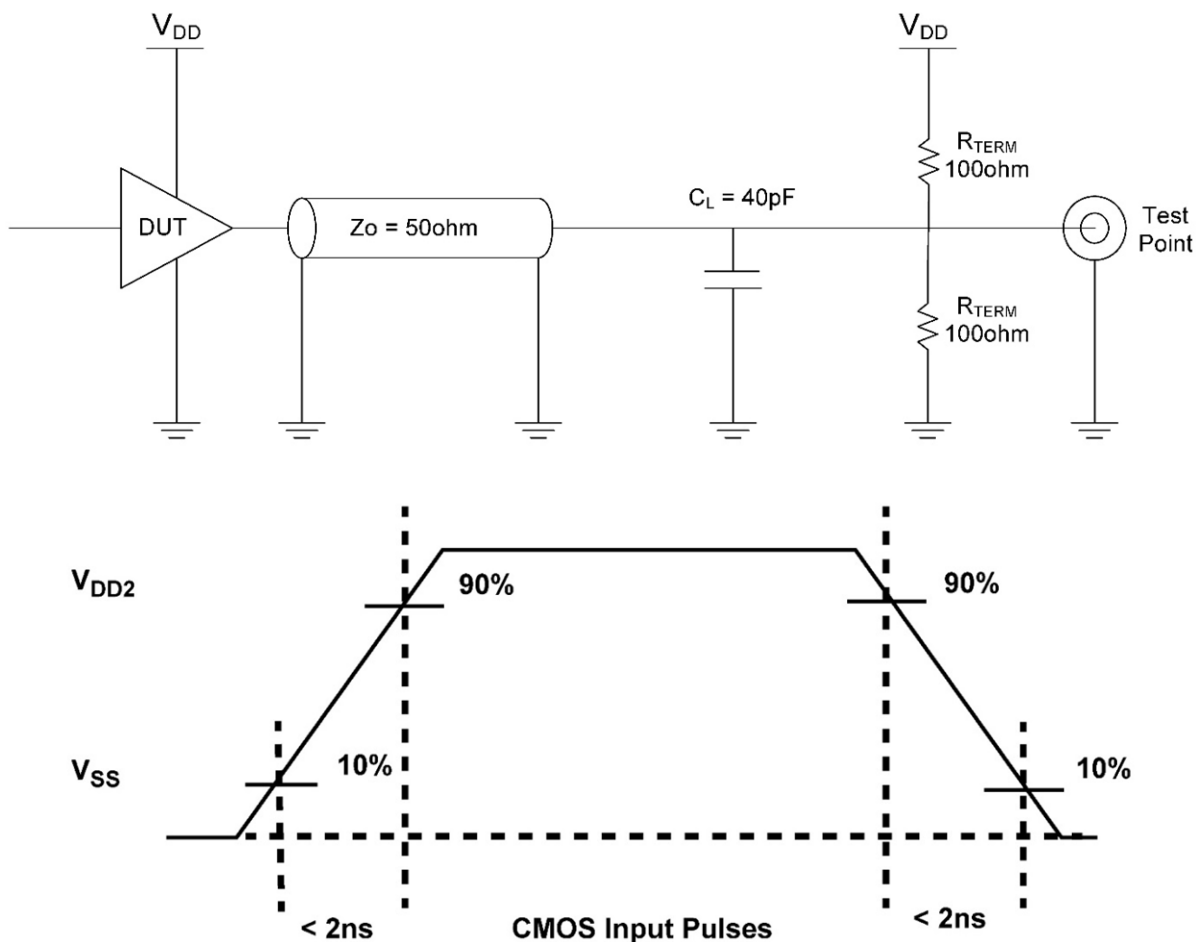
# UT8ER1M32, UT8ER2M32, UT8ER4M32



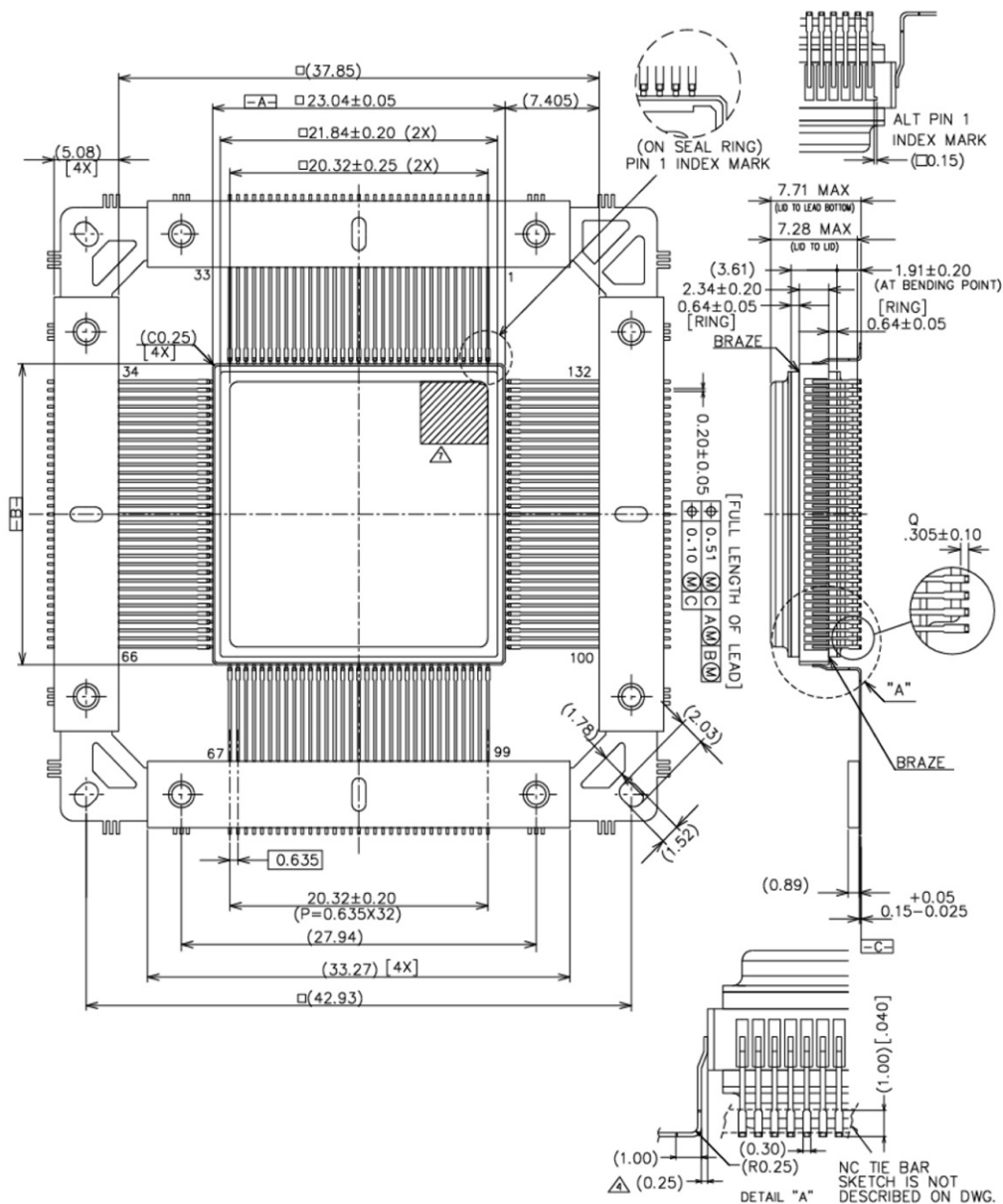Figure 8. AC Test Loads and Input Waveforms

**Notes**:
1) Measurement of data output occurs at the low to high or high to low transition mid-point (i.e., CMOS input = $V_{DD2}/2$)

32, 64, 128 Megabit SRAM MCM

# UT8ER1M32, UT8ER2M32, UT8ER4M32

**Packaging**



Figure 9. 132-Lead Side-Brazed Dual Cavity Ceramic Quad Flatpack

**Notes**:

1) Package Material: Opaque 90% minimum alumina ceramic.
2) All exposed metal areas must be gold plated 2.5um to 5.7um thick over electroplated nickel undercoating 2.5um to 8.9um thick per MIL-PRF-38535.
3) The seal ring is electrically connected to VSS.
4) Dogleg geometries optional within dimensions shown.
5) Tiebar may have excize slots of various. Configurations and are vendor option.
6) Circled letter are for CAES use only.
7) Package mark will include a dot to indicate. The pin 1 corner within the area shown
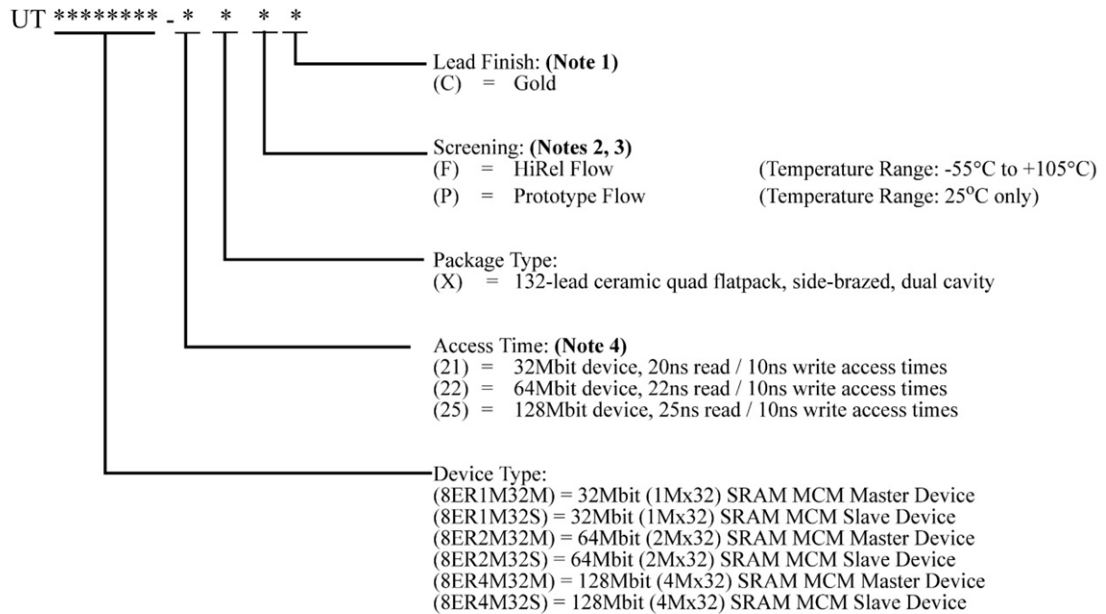
32, 64, 128 Megabit SRAM MCM

# UT8ER1M32, UT8ER2M32, UT8ER4M32

## Ordering Information

**32Mbit (1Mx32) SRAM MCM**

**64Mbit (2Mx32) SRAM MCM**

**128Mbit (4Mx32) SRAM MCM**

UT ******** - * * * *

**Lead Finish: (Note 1)**
(C)  =  Gold

**Screening: (Notes 2, 3)**
(F)  =  HiRel Flow          (Temperature Range: -55°C to +105°C)
(P)  =  Prototype Flow      (Temperature Range: 25°C only)

**Package Type:**
(X)  =  132-lead ceramic quad flatpack, side-brazed, dual cavity

**Access Time: (Note 4)**
(21)  =  32Mbit device, 20ns read / 10ns write access times
(22)  =  64Mbit device, 22ns read / 10ns write access times
(25)  =  128Mbit device, 25ns read / 10ns write access times

**Device Type:**
(8ER1M32M) = 32Mbit (1Mx32) SRAM MCM Master Device
(8ER1M32S) = 32Mbit (1Mx32) SRAM MCM Slave Device
(8ER2M32M) = 64Mbit (2Mx32) SRAM MCM Master Device
(8ER2M32S) = 64Mbit (2Mx32) SRAM MCM Slave Device
(8ER4M32M) = 128Mbit (4Mx32) SRAM MCM Master Device
(8ER4M32S) = 128Mbit (4Mx32) SRAM MCM Slave Device

**Notes:**

1) Lead finish is "C" (Gold) only.
2) Prototype Flow per CAES Manufacturing Flows Document. Devices are tested at 25°C only. Lead finish is GOLD "C" only. Radiation is neither tested nor guaranteed.
3) HiRel flow per CAES Manufacturing Flows Document. Radiation is neither tested nor guaranteed.
4) Device option (21) is applicable to 32Mbit device types only. Option (22) is applicable to 64Mbit device types only. Option (25) is applicable to 128Mbit device types only.
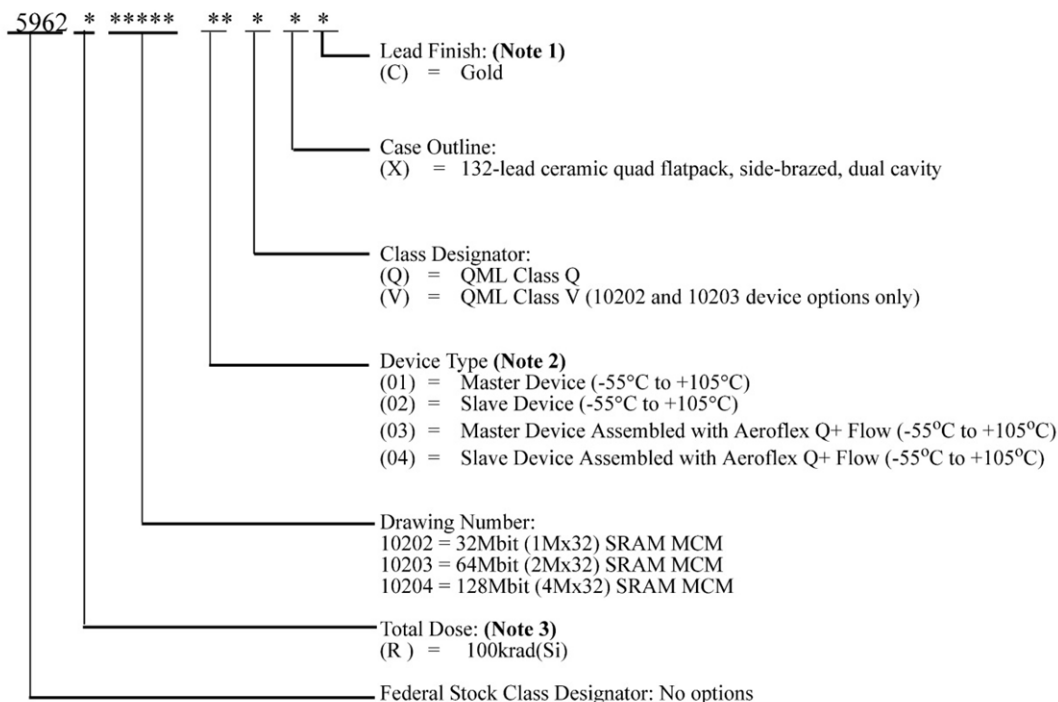
32, 64, 128 Megabit SRAM MCM

# UT8ER1M32, UT8ER2M32, UT8ER4M32

**32Mbit (1Mx32) SRAM MCM: SMD**

**64Mbit (2Mx32) SRAM MCM: SMD**

**128Mbit (4Mx32) SRAM MCM: SMD**

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**Lead Finish: (Note 1)**
(C) = Gold

**Case Outline:**
(X) = 132-lead ceramic quad flatpack, side-brazed, dual cavity

**Class Designator:**
(Q) = QML Class Q
(V) = QML Class V (10202 and 10203 device options only)

**Device Type (Note 2)**
(01) = Master Device (-55°C to +105°C)
(02) = Slave Device (-55°C to +105°C)
(03) = Master Device Assembled with Aeroflex Q+ Flow (-55°C to +105°C)
(04) = Slave Device Assembled with Aeroflex Q+ Flow (-55°C to +105°C)

**Drawing Number:**
10202 = 32Mbit (1Mx32) SRAM MCM
10203 = 64Mbit (2Mx32) SRAM MCM
10204 = 128Mbit (4Mx32) SRAM MCM

**Total Dose: (Note 3)**
(R) = 100krad(Si)

**Federal Stock Class Designator:** No options

**Notes:**
1) Lead finish is "C" (Gold) only.
2) CAES's Q+ assembly flow, as defined in section 4.2.2.d of the SMD, provides QML-Q product through the SMD that is manufactured with CAES's standard QML-V flow.
3) TID tolerance guarantee of 1E5 is tested in accordance with MIL-STD-883 Test Method 1019 (condition A and section 3.11.2) resulting in an effective dose rate of 1 rad (Si)/sec.

32, 64, 128 Megabit SRAM MCM

# UT8ER1M32, UT8ER2M32, UT8ER4M32

## Revision History

| Revision Date | Description of Change | Page(s) | Author |
|---|---|---|---|
| 6/15 | Added new datasheet format | All | Leslie |
| 12/15 | Added new Table 1, edited Master and Slave Mode AC Characteristics, and updated export disclaimer | 4, 23, 28 | Leslie |
| 2/18 | Edited Read Cycle text, Added parameters to DC and AC Characteristic tables, Edited Absolute Maximum, Replaced package drawing to correct lid height | 9, 13, 14, 15, 12, 25 | Nelson |
| 7/21 | Corrected table 2 pinout for UT8ER4M32M and UT8ER4M32S columns for pin 45 and 46 which were NC but should have been #E7 and #E5 respectively | 5 | Leslie |

# UT8ER1M32, UT8ER2M32, UT8ER4M32

## Datasheet Definitions

| | DEFINITION |
|---|---|
| Advanced Datasheet | CAES reserves the right to make changes to any products and services described herein at any time without notice.  The product is still in the development stage and the datasheet **is subject to change**. Specifications can be **TBD** and the part package and pinout are **not final**. |
| Preliminary Datasheet | CAES reserves the right to make changes to any products and services described herein at any time without notice.  The product is in the characterization stage and prototypes are available. |
| Datasheet | Product is in production and any changes to the product and services described herein will follow a formal customer notification process for form, fit or function changes. |

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