APPLICATION NOTE

RELEASED 6/17

UT8MR2M8 16M and UT8MR8M8 64M MRAMs

Q1)
Why is the maximum storage temperature 125°C while the maximum junction temperature is 150°C?

A1)
The maximum junction temperature represents a transient condition as opposed to the maximum storage temperature which implies an indefinite time. In order to maintain the highest reliability for data integrity the device should not be exposed to temperatures above 125°C for an indefinite period of time.

Q2)
Can MRAM be used as a replacement for EEPROMs or other non-volatile memory?

A2)
Yes, the CAES MRAM solution offers a functional upset immune alternative to commercial and other RadTolerant devices utilizing a simple asynchronous 8bit data bus interface. The MRAM provides a securer radiation solution over floating gate architectures as the MRAM technology does not require internal high voltage for programming which is susceptible to ion strike failures. Additionally, the MRAM utilizes symmetrical read write access cycle times similar to SRAMs eliminating the long page by page microsecond write cycles of floating gate designs.

Q3)
Are IBIS models available for both 16M & 64M MRAM?

A3)
Yes, IBIS models are available for download from the CAES Microelectronics HiRel Memories product page website: cobhamaes.com.

There is a model for the 16M, 64M and an early version prototype for the 64M. This version of product (64M prototype) did not include the enable all control input signal and multi bit error (MBE) output function.

Q4)
Does the MRAM device employ an error correction scheme?

A4)
Yes, the MRAMs 16M and 64M Multichip Module (MCM), employ an ECC (error correcting code) function. Every read activity compares data to stored coded data. Single bit transient errors are corrected autonomously. The ECC operation is transparent to the user. Since the MRAM core is immune to upsets, only transient errors occur, and therefore a write back function is not necessary.

Q4)
Is the MRAM SEFI immune?

A4)
No, SEFIs were observed during heavy ion testing. The SEFI rate is predicted in the single digit range per 15 year mission depending on conditions and orbit. For more specifics, contact factory for SEE test report and reference application note: SEFI Work-Arounds for MRAM Devices on the CAES Microelectronics HiRel Memories product page website: cobhamaes.com

APPLICATION NOTE

RELEASED 6/17

UT8MR2M8 16M and UT8MR8M8 64M MRAMs

The CAES MRAM devices were intended to be used as boot loader or configuration memory. Using the MRAM as a persistent application memory such as an SRAM without the capability of detecting data errors is not recommended. The MRAM provides a ZZ/RST pin for SEFI recovery on the rare occasion one is detected.

Q5)
What is the ZZ/RST pin and why is it needed?

A5)
The ZZ/RST pin serves two purposes. The first provides a low power down sleep mode for boot loader applications where the device is likely to experience long periods on inactivity. The second provides a reset capability in the rare event a SEFI is detected as discussed in Q&A #4. For more specifics on the ZZ/RST pin functionality, reference the device datasheets on the CAES Microelectronics HiRel Memories product page website: cobhamaes.com

Q6)
What is the value of the internal pull down on the ZZ/RST input pin?

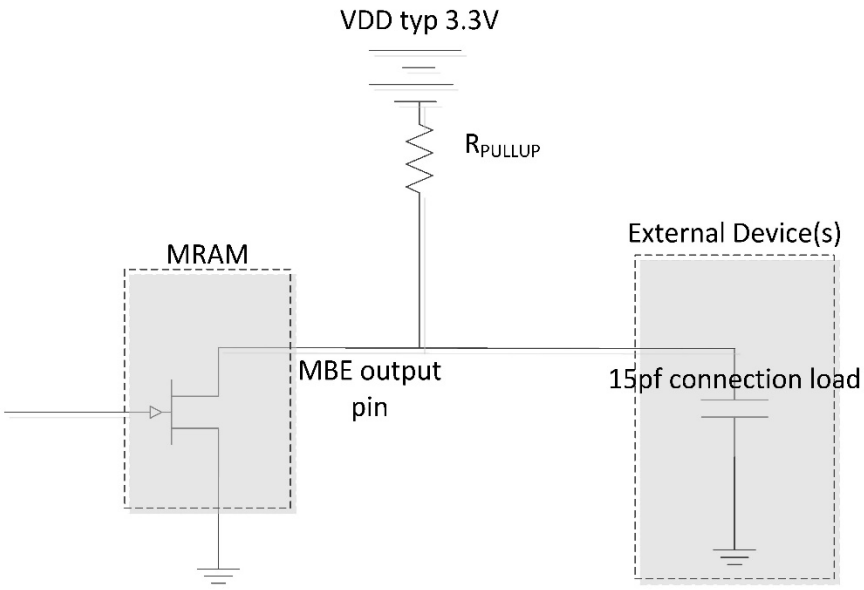
A6)
The ZZ/RST pin is internally designed with an active 50uA pull down.

Q7)
The 64M device has an MBE pin. What is the purpose of the MBE pin?

A7)
The MBE pin is an output which provides the user notification that corrupt data exist. In the unlikely event that a multiple bit transient upset occurs during a read operation of the 64M MRAM device, the MBE output will drive low during the data valid time of that read cycle. The MBE output pin is only valid after tELQV or tAVQV minimum data access times (50ns) have been satisfied. Spurious MBE low pulses can occur at the initiation of any read cycle, but these are not valid unless they persist beyond the 50ns minimum read access time of tAVQV or tELQV. It is suggested that users poll the MBE pin at the same time the data is being polled.

Additionally, the MBE output requires an initialization (chip enable assertion) of all die within the MCM package after a power up or reset event as described in the device datasheet. The MBE pin is an open drain output pin which requires an external pullup to reach the high inactive state. The value of the pullup required depends on the circuit load of the application. It may be important for the signal to reach the VIH input level of any connected logic devices within the data polling time of the application. The simplified calculation for R_{PULLUP} is shown below:

UT8MR2M8 16M and UT8MR8M8 64M MRAMs



Assumption: VDD = 3.3V, VIH = 0.7 x VDD, Vc initial = 0V
Application Variables: t = access time of application C = capacitive loading of external device(s) and MRAM

When MBE is not driving low, the signal to external device(s) needs to be pulled up by an external pullup resistor. The time it takes to pull the signal high can be calculated using the capacitive charging equation $Vc = E\ (1-e^{-t/RC})$
Example: Requirement is for Vc reach VIH min by required polling time (50ns)
Vc = MBE pin voltage as a function of time
E = VDD, C = capacitive loading of external device(s) + output load of MRAM (60pf)
R = value of R_{PULLUP}
Since VIH is typically 70% VDD, $(1-e^{-t/RC}) = 0.7$
Therefore: R = –t / C ln(0.3); and R = –50ns / 75pf ln(0.3) = 554ohms

Q8)
Are there any special handling requirements for MRAMs during the assembly or testing process?

A8)
Yes, please refer to our MRAM Magnetic Immunity application note on the CAES Microelectronics HiRel Memories product page website: cobhamaes.com

Q9)
What is the export classification for CAES MRAMs?

A9)
This product is classified as 9A515.e.2.

APPLICATION NOTE

RELEASED 6/17

UT8MR2M8 16M and UT8MR8M8 64M MRAMs

Q10)
Can the MRAM interface directly with the LEON 3FT PROM memory port?

A10)
Yes, the MRAM uses the same asynchronous controls and interface as CAES's 256K PROM, and is a functional equivalent to most standard 8 bit parallel asynchronous devices. Additionally, the MRAM has equivalent read access times to most industry available PROMs. The MRAM has symmetrical write and read cycle times, unlike other non-volatile memory technologies.

Q11)
Can the MRAM be used to configure the Virtex FPGAs?

A11)
Yes, the 64Mb MRAM can be used to configure the Xilinx Virtex-5 FPGA FX130. The FX130 (SIRF, XQR5V) is the largest space qualified FPGA from Xilinx. The 64Mb MCM, or a combination of 16Mb MRAMs, can be used with the smaller XQR4V (Virtex-4) devices. Please reference application note; Programming the 64Mbit MRAM for Configuring Xilinx Virtex-5 FPGA on the CAES Microelectronics HiRel Memories product page website: cobhamaes.com

Q12)
What are the masses of the MRAM products and do the MRAM packages (16M and 64M) require thermal or structural bonding or staking to a printed circuit card assembly?

A12)
16M 40 pin FP (25mil) pitch = 6.48g, 40 pin FP (50mil) pitch = 7.92 (w/o carrier) 64M 64 pin FP = 21.99g
CAES does not make recommendation on device lead forming or component mounting processes. Customer's circuit card assembly engineers need to determine the best methods for device mounting for their given set of specifications. It is noted however that the MRAM is a very low power device which typically uses < ¼ W under maximum operating speed therefore; thermal bonding is not a necessity from the device's heat dissipation perspective.

Q13)
When were the CAES MRAMs qualified and were Aerospace Corporation and DLA Involved in the qualification process?

A13)
Yes, Aerospace and DLA have reviewed and approved CAES's MRAM qualification approach. CAES has a long history of QML qualifications working with Aerospace Corporation and DLA. QMLV certification for the 16M MRAM was obtained December, 2015 and the 64M MRAM was obtained January, 2016.

UT8MR2M8 16M and UT8MR8M8 64M MRAMs

Q14)
Did CAES included their usual excellent level of "new technology insertion", including collaboration with Aerospace Corporation for concurrence on Failure Mode and Effects as part of the Reliability Assessment for their MRAM?

A14)
Yes. CAES conducted a full FMEA evaluation in collaboration with Aerospace Corporation and DLA throughout the design, package development, assembly, and test of this product.

Q15)
Does the MRAM utilize a write protection function?

A15)
The MRAM does not provide a programmable block or write protect scheme, but it does have a write enable (/W) control pin which can be pulled high in OTP (one time programmable) applications. Additionally, the MRAM features a low voltage write inhibit circuit which protects the data from corruption due to inadvertent write should the device power drop below the specified value. Reference the device datasheet for details of write inhibit operations.

Q16)
Can the MRAM device be programmed off board?

A16)
While most applications use in-system programming by writing address and data to the device, off board programming is supported by BP Microsystems for the 16Mb MRAM only. Please visit their website http://www.bpmmicro.com/ for details.